GR2DS8BD-2GBXXX / GR2DS8BD-1GBXXX / GR2DS6BD-512XXX

DDR2 2GB, 1GB, 512MB 2Ranks SODIMM

GENERAL DESCRIPTION

The Gigaram **GR2DS8BD-2GBXXX, GR2DS8BD-1GBXXX and GR2DS6BD-512XXX** are 256M bit x 64, 128M bit x 64 and 64M bit x 64 DDR2 SDRAM high density JEDEC standard SODIMM. They are consists of sixteen or eight CMOS 128Mx8 DDR2 SDRAMs for 2GB, 64Mx8 DDR2 SDRAMs for 1GB and 32Mx16 DDR2 SDRAMs for 512MB in 60/68 ball FBGA packages, mounted on a 200Pin glass-epoxy substrate.

DDR2 REGISTERED DIMM PART INFORMATION

Part Number	Density	Organization	Component	Rank	Height
GR2DS8BD-2GB800/667/533/400	2GB	256Mx64	128Mx8 * 16	2	1.181 Inch
GR2DS8BD-1GB800/667/533/400	1GB	128Mx64	64Mx8 * 16	2	1.181 Inch
GR2DS6BD-512800/667/533/400	512MB	64Mx64	32Mx16 * 8	2	1.181 Inch

FEATURES

- Performance range

Part Number	DDR2-800	DDR2-667	DDR2-533	DDR2-400	Unit
Speed @ CL3	400	400	400	400	Mbps
Speed @ CL4	533	533	533	400	Mbps
Speed @ CL5	800	667	533	-	Mbps
Speed @ CL6	-	-	-	-	Mbps
CL-tRCD-tRP	5-5-5	5-5-5	4-4-4	3-3-3	CK

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8 ± 0.1V
- 200Mhz f_{CK} for 400Mb, 267Mhz f_{CK} for 533Mb, 333Mhz f_{CK} for 667Mb, 400Mhz f_{CK} for 800Mb/sec/pin
- 4 Bank, 8 Bank
- Posted /CAS
- Programmable /CAS Latency: 3, 4, 5
- Write Latency (WL) = Read Latency (RL) -1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60/68 ball FBGA – 128Mx8, 64Mx8, 32Mx16
- All of Lead-Free products are compliant for RoHS

ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
32Mx16 (512Mb) based module	A0-A12	A0-A9	BA0-BA1	A10
64Mx8 (512Mb) based module	A0-A13	A0-A9	BA0-BA1	A10
128Mx8 (1Gb) based module	A0-A13	A0-A9	BA0-BA2	A10

PIN CONFIGURATIONS (Front Side/ Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	2	V_{SS}	51	DQ2	52	DM2	101	A1	102	A0	151	DQ42	152	DQ46
3	V_{SS}	4	DQ4	53	V_{SS}	54	V_{SS}	103	V_{DD}	104	V_{DD}	153	DQ43	154	DQ47
5	DQ0	6	DQ5	55	DQ18	56	DQ22	105	A10	106	BA1	155	V_{SS}	156	V_{SS}
7	DQ1	8	V_{SS}	57	DQ19	58	DQ23	107	BA0	108	/RAS	157	DQ48	158	DQ52
9	V_{SS}	10	DM0	59	V_{SS}	60	V_{SS}	109	/WE	110	/SO	159	DQ49	160	DQ53
11	/DQS0	12	V_{SS}	61	DQ24	62	DQ28	111	V_{DD}	112	V_{DD}	161	V_{SS}	162	V_{SS}
13	DQS0	14	DQ6	63	DQ25	64	DQ29	113	/CAS	114	ODT0	163	TEST	164	CK1
15	V_{SS}	16	DQ7	65	V_{SS}	66	V_{SS}	115	/S1	116	A13	165	V_{SS}	166	/CK1
17	DQ2	18	V_{SS}	67	DM3	68	/DQS3	117	V_{DD}	118	V_{DD}	167	/DQS6	168	V_{SS}
19	DQ3	20	DQ12	69	NC	70	DQS3	119	ODT1	120	NC	169	DQS6	170	DM6
21	V_{SS}	22	DQ13	71	V_{SS}	72	V_{SS}	121	V_{SS}	122	V_{SS}	171	V_{SS}	172	V_{SS}
23	DQ8	24	V_{SS}	73	DQ26	74	DQ30	123	DQ32	124	DQ36	173	DQ50	174	DQ54
25	DQ9	26	DM1	75	DQ27	76	DQ31	125	DQ33	126	DQ37	175	DQ51	176	DQ55
27	V_{SS}	28	V_{SS}	77	V_{SS}	78	V_{SS}	127	V_{SS}	128	V_{SS}	177	V_{SS}	178	V_{SS}
29	/DQS1	30	CK0	79	CKE0	80	NC/CKE1	129	/DQS4	130	DM4	179	DQ56	180	DQ60
31	DQS1	32	/CK0	81	V_{DD}	82	V_{DD}	131	DQS4	132	V_{SS}	181	DQ57	182	DQ61
33	V_{SS}	34	V_{SS}	83	NC	84	NC	133	V_{SS}	134	DQ38	183	V_{SS}	184	V_{SS}
35	DQ10	36	DQ14	85	BA2	86	NC	135	DQ34	136	DQ39	185	DM7	186	/DQS7
37	DQ11	38	DQ15	87	V_{DD}	88	V_{DD}	137	DQ35	138	V_{SS}	187	V_{SS}	188	DQS7
39	V_{SS}	40	V_{SS}	89	A12	90	A11	139	V_{SS}	140	DQ44	189	DQ58	190	V_{SS}
41	V_{SS}	42	V_{SS}	91	A9	92	A7	141	DQ40	142	DQ45	191	DQ59	192	DQ62
43	DQ16	44	DQ20	93	A8	94	A6	143	DQ41	144	V_{SS}	193	V_{SS}	194	DQ63
45	DQ17	46	DQ21	95	V_{DD}	96	V_{DD}	145	V_{SS}	146	/DQS5	195	SDA	196	V_{SS}
47	V_{SS}	48	V_{SS}	97	A5	98	A4	147	DM5	148	DQS5	197	SCL	198	SA0
49	/DQS2	50	NC	99	A3	100	A2	149	V_{SS}	150	V_{SS}	199	V_{DDSPD}	200	SA1

PIN DESCRIPTION

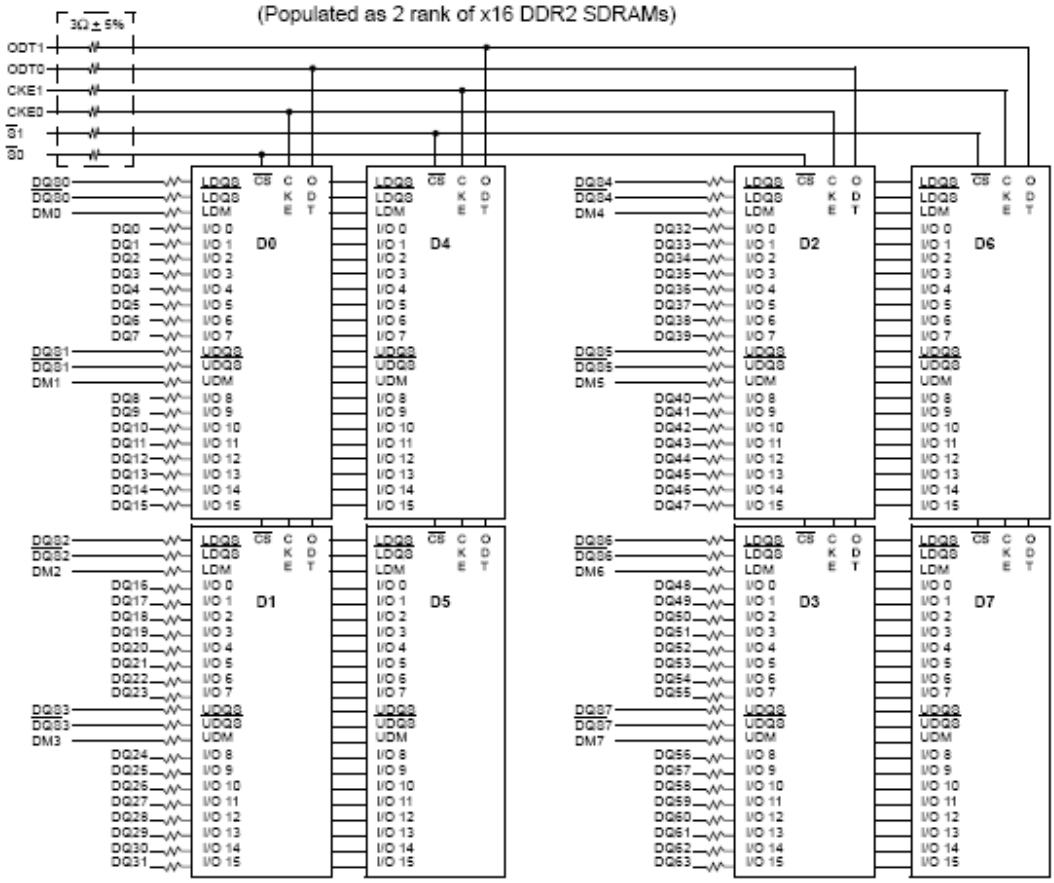
PIN NAME	DESCRIPTION	PIN NAME	DESCRIPTION
CK0, CK1	Clock Inputs, positive line	SDA	SPD Data Input/Output
/CK0, /CK1	Clock Inputs, negative line	SA0, SA1	SPD Address
CKE0, CKE1	Clock Enables	DQ0-DQ63	Data Input/Output
/RAS	Row Address Strobe	DM0-DM7	Data Masks
/CAS	Column Address Strobe	DQS0-DQS7	Data Strobes
/WE	Write Enables	/DQS0-/DQS7	Data strobes, negative line
/S0, /S1	Chip Selects	TEST	Memory bus test tool
A0-A9, A11-A13	Address Inputs	V_{DD}	Core and I/O Power
A10/AP	Address Inputs/Autoprecharge	V_{SS}	Ground
BA0 - BA2	SDRAM Bank Address	V_{REF}	Input/Output Reference
ODT0, ODT1	On die Termination	V_{DDSPD}	SPD Power
SCL	SPD Clock Input	NC	No Connect

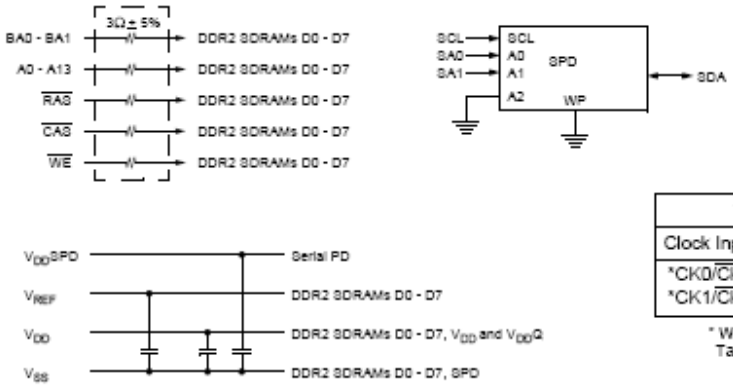
* The V_{DD} and V_{DDQ} pins are tied to the single power-plane on PCB.

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

SYMBOL	TYPE	FUNCTION
CK0-CK1 /CK0-/CK1	Input	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling of /CK. A delay Locked Loop (DLL) circuit is driven from the clock input and the output timing for read operations is synchronized to the input clock.
CKE0-CKE1	Input	Activates the DDR2 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
/S0-/S1	Input	Enables the associated SDRAM command decoder when low and disable decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by /SO, Rank 1 is selected by /S1. Ranks are also called “Physical banks”
/RAS, /CAS, /WE	Input	When sampled at the positive rising edge of the clock, /CAS, /RAS and /WE define the operation to be executed by the SDRAM.
BA0-BA2	Input	Selects which DDR2 SDRAM internal bank is activated.
ODT0-ODT1	Input	Asserts on-die termination for DQ, DM, DQS and /DQS signals if enabled via the DDR2 SDRAM Extended Mode Register Set (EMRS)
A0-A9, A10/AP, A11-A13	Input	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn. If AP is low, BA0-BAn are used to define which bank to precharge.
DQ0-DQ63	In/Out	Data Input/Output pins
DM0-DM7	Input	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect..
DQS0-DQS7 /DQS0-/DQS7	In/Out	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR2 SDRAMs and is sent at the leading edge of the data window. /DQS signals are complements, and timing is relative to the crosspoint of respective DQS and /DQS if the module is to be operated in single ended strobe mode, all /DQS signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
V_{DD}, V_{DDSPD}, V_{SS}	Supply	Power supplies for core, I/O, Serial Presence Detect and ground for the module.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} to act as a pullup.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A register may be connected from the SCL bus time to V_{DDSPD} to act as a pullup.
SA0-SA1	Input	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
TEST	In/Out	Used by memory bus analysis tools (unused on memory DIMMs)

FUNCTIONAL BLOCK DIAGRAM: 512MB (64Mx64) MODULE



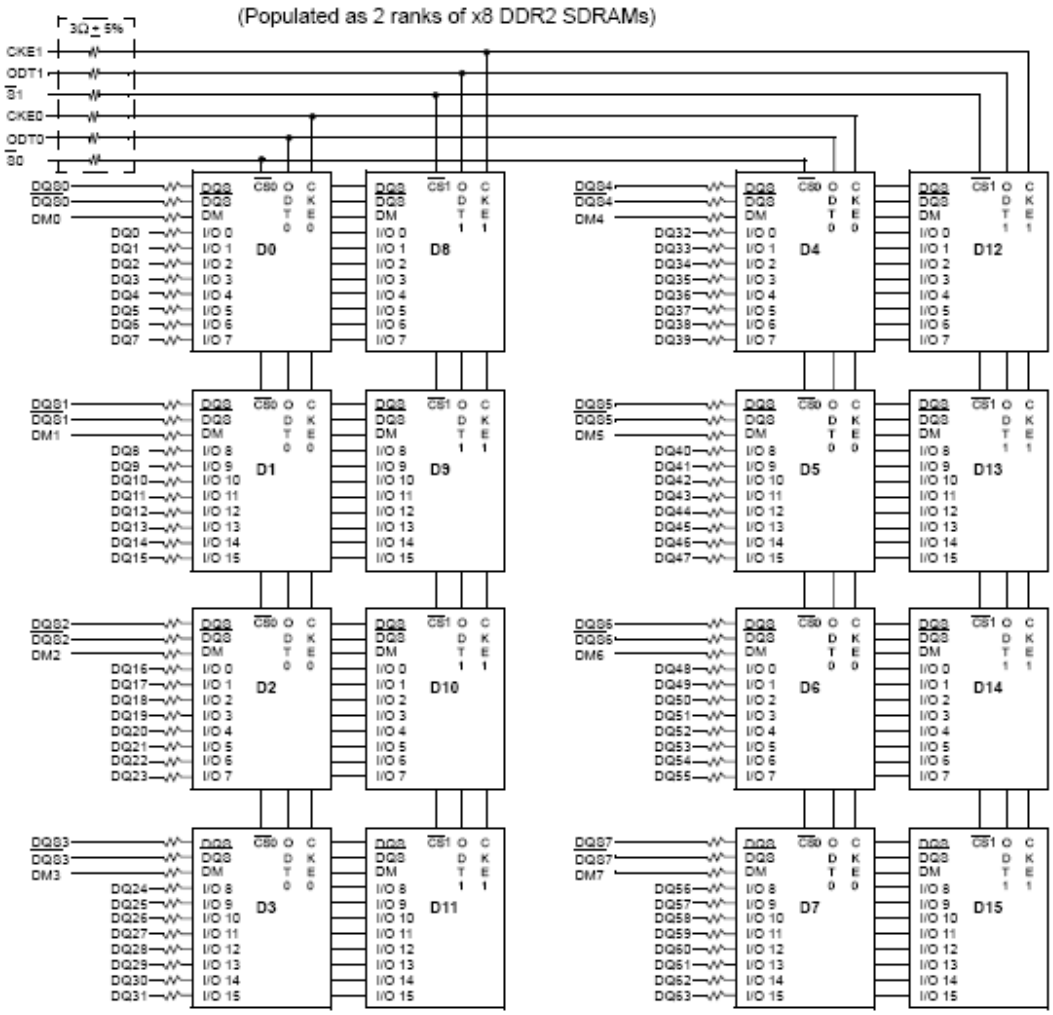


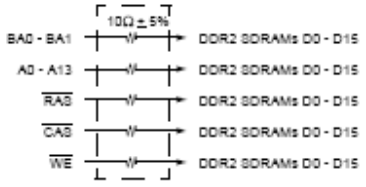
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	4 DDR2 SDRAMs
*CK1/$\overline{CK1}$	4 DDR2 SDRAMs

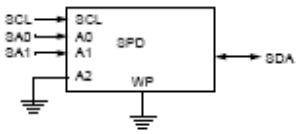
* Wire per Clock Loading Table/Wiring Diagrams

Note :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3.0 Ohms ± 5%.

FUNCTIONAL BLOCK DIAGRAM: 1GB (128Mx64) MODULE

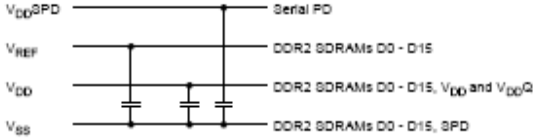






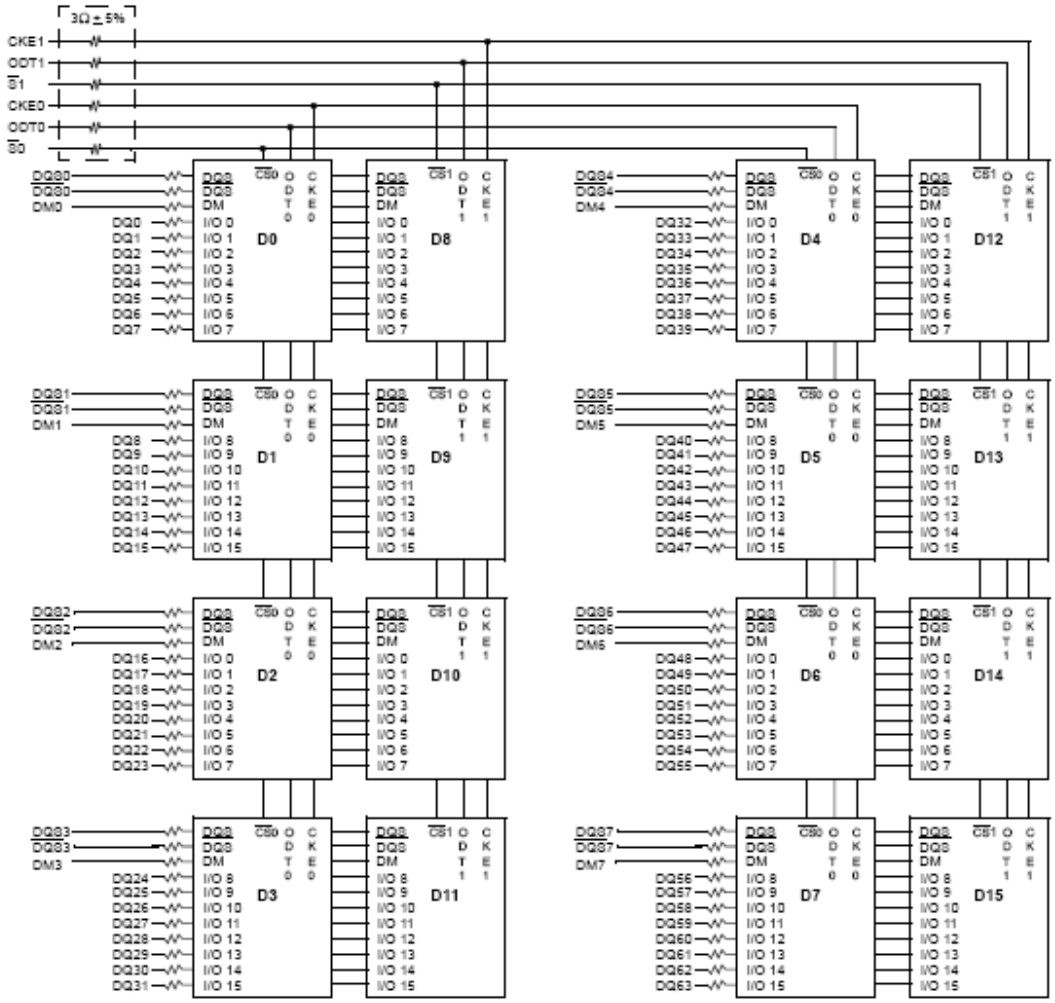
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	8 DDR2 SDRAMs
*CK1/$\overline{CK1}$	8 DDR2 SDRAMs

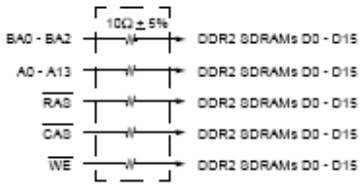
* Wire per Clock Loading Table/Wiring Diagrams

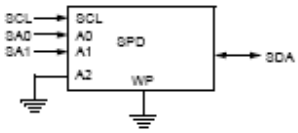


Note :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 10.0 Ohms ± 5%.

FUNCTIONAL BLOCK DIAGRAM: 2GB (256Mx64) MODULE







* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	8 DDR2 SDRAMs
*CK1/CK1	8 DDR2 SDRAMs

* Wire per Clock Loading Table/Wiring Diagrams

Note :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 10.0 Ohms ± 5%.

ABSOLUTE MAXIMUM DC RATINGS

Parameter	Symbol	Limit Values		Unit	Note
		Min.	Max.		
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	2.3	V	1
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-0.5	2.3	V	1
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5	2.3	V	1
Voltage on V_{DDL} relative to V_{SS}	V_{DDL}	-0.5	2.3	V	1
Storage temperature range	T_{STG}	-55	+100	° C	1, 2

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC OPERATING CONDITIONS

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Norm.	Max.		
DDR2 SDRAM Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Supply Voltage for DLL	V_{DDL}	1.7	1.8	1.9	V	4
Core Supply Voltage	V_{DDSPD}	1.7	-	3.6	V	5
Supply Voltage Output	V_{DDQ}	1.7	1.8	1.9	V	4
Input Reference Voltage	V_{REF}	0.49* V_{DDQ}	0.50* V_{DDQ}	0.51*V_{DDQ}	mV	1, 2
Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

Note: There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed +/-2% VREF(DC).
3. VTT of transmitting device must track VREF of receiving device.
4. AC parameters are measured with VDD, VDDQ and VDDL tied together.
5. SODIMMs that include an optional temperature sensor may require a restricted VDDSPD operating voltage range for proper operation of the temperature sensor. Refer to the thermal sensor specification for details regarding the supported voltage range. All other functions of the SO-DIMM SPD are supported across the full VDDSPD range.

OPERATING TEMPERATURE RANGE

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Operating Temperature	TOPER	0	+95	° C	1, 2

Note:

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

INPUT DC LOGIC LEVELS

Parameter	Symbol	MIN	MAX	Units	Notes
DC Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 125	V_{DDQ} + 300	mV	
DC Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-300	V_{REF} - 125	mV	

INPUT AC LOGIC LEVELS

Parameter	Symbol	MIN	MAX	Units	Notes
AC Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 250	-	mV	
AC Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 250	mV	

OPERATING CURRENT TABLE

64Mx64 512MB MODULE

Symbol	DDDR2-800@CL5	DDR2-667@CL5	DDR2-533@CL4	DDR2-400@CL3	Unit	Note
I_{DD0}	540	520	500	500	mA	1
I_{DD1}	620	600	560	560	mA	1
I_{DD2P}	64	64	64	64	mA	2
I_{DD2Q}	280	280	240	240	mA	2
I_{DD2N}	320	320	280	280	mA	2
$I_{DD3P(F)}$	240	20	240	240	mA	2
$I_{DD3P(S)}$	96	96	96	96	mA	2
I_{DD3N}	400	380	340	340	mA	2
I_{DD4W}	700	640	560	540	mA	1
I_{DD4R}	920	840	700	680	mA	1
I_{DD5B}	620	600	580	580	mA	2
I_{DD6}	64	64	64	64	mA	2
I_{DD7}	1280	1120	1100	1000	mA	1

128Mx64 1GB MODULE

Symbol	DDDR2-800@CL5	DDR2-667@CL5	DDR2-533@CL4	DDR2-400@CL3	Unit	Note
I_{DD0}	1000	920	880	840	mA	1
I_{DD1}	1080	1040	960	960	mA	1
I_{DD2P}	128	128	128	128	mA	2
I_{DD2Q}	560	560	480	480	mA	2
I_{DD2N}	640	640	560	560	mA	2
$I_{DD3P(F)}$	480	480	480	480	mA	2
$I_{DD3P(S)}$	192	192	192	192	mA	2
I_{DD3N}	800	760	680	680	mA	2
I_{DD4W}	1240	1160	1000	960	mA	1
I_{DD4R}	1480	1400	1160	1080	mA	1
I_{DD5B}	1240	1200	1160	1120	mA	2
I_{DD6}	128	128	128	128	mA	2
I_{DD7}	2040	1760	1720	1720	mA	1

256Mx64 2GB MODULE

Symbol	DDDR2-800@CL5	DDR2-667@CL5	DDR2-533@CL4	DDR2-400@CL3	Unit	Note
I_{DD0}	1120	1040	1000	960	mA	1
I_{DD1}	1200	1120	1080	1040	mA	1
I_{DD2P}	240	240	240	240	mA	2
I_{DD2Q}	720	720	720	640	mA	2
I_{DD2N}	800	720	720	640	mA	2
$I_{DD3P(F)}$	720	640	560	560	mA	2
$I_{DD3P(S)}$	288	288	288	288	mA	2
I_{DD3N}	920	840	840	760	mA	2
I_{DD4W}	1800	1600	1400	1240	mA	1
I_{DD4R}	1880	1600	1480	1280	mA	1
I_{DD5B}	1880	1800	1760	1680	mA	2
I_{DD6}	240	240	240	240	mA	2
I_{DD7}	2800	2600	2440	2240	mA	1

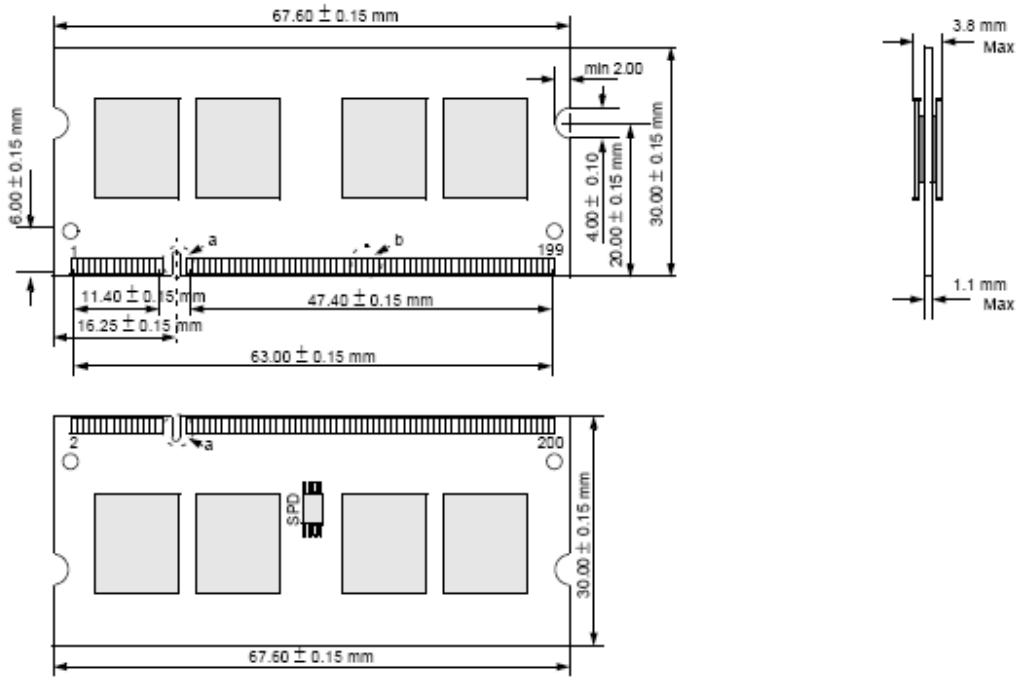
* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

INPUT/OUTPUT CAPACITANCE

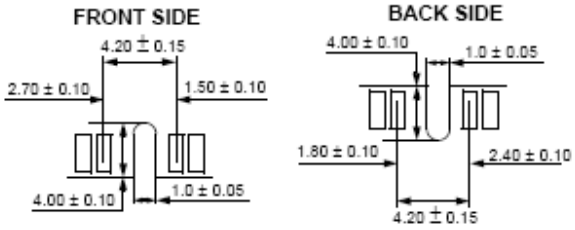
(V_{DD}=1.8V, V_{DDQ}=1.8V, TA=25°C)

Parameter	Symbol	Min	Max	Units
Input Capacitance, CK and /CK	CCK	-	48	
Input Capacitance, CKE, /CS, Addr, /RAS, /CAS, /WE	CI	-	42	pF
Input Capacitance, DQ, DM, DQS, /DQS	CIO	-	10	

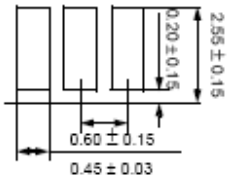
PACKAGE DIMENSION (Unit: mm): 32Mx16 based 64Mx64 MODULE



DETAIL a



DETAIL b



PACKAGE DIMENSION (Unit: mm): 64Mx8 / 128Mx8 based 128Mx64 / 256Mx64 MODULE