

## DDR2 4GB 2 RANKS ECC REGISTERED DIMM

## GENERAL DESCRIPTION

The Gigaram **GR2DR4BD-E4GBXXX** is ECC Registered Dual-Die DIMM with 1.25inch (30.00mm) height based on DDR2 technology. DIMMs are available as ECC modules in 512Mx72 (4GByte) organization and density, intended for mounting into 240-Pin connector sockets. The memory array is designed with 36pcs of 256Mx4 DDR2 SDRAMs. All control and address signals are re-driven on the DIMM using register devices and a PLL for the clock distribution. This reduces capacitive loading to the system bus, but adds one cycle to the SDRAM timing. Double capacitors are mounted on the PCB board.

## DDR2 ECC REGISTERED DIMM PART INFORMATION

Part Number	Density	Organization	Component	Rank	Height
<b>GR2DR4BD-E4GB800</b>	4GB	512MX72	256Mx4 * 36	2	1.25 Inch
<b>GR2DR4BD-E4GB667</b>	4GB	512MX72	256Mx4 * 36	2	1.25 Inch
<b>GR2DR4BD-E4GB533</b>	4GB	512MX72	256Mx4 * 36	2	1.25 Inch
<b>GR2DR4BD-E4GB400</b>	4GB	512MX72	256Mx4 * 36	2	1.25 Inch

## FEATURES

- Performance range

Part Number	DDR2-800	DDR2-667	DDR2-533	DDR2-400	Unit
Speed @ CL3	-	400	400	400	Mbps
Speed @ CL4	533	533	533	400	Mbps
Speed @ CL5	667	667	-	-	Mbps
Speed @ CL6	800	-	-	-	Mbps
CL-tRCD-tRP	6-6-6	5-5-5	4-4-4	3-3-3	CK

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8 ± 0.1V
- 200Mhz f<sub>CK</sub> for 400Mb, 267Mhz f<sub>CK</sub> for 533Mb, 333Mhz f<sub>CK</sub> for 667Mb, 400Mhz f<sub>CK</sub> for 800Mb/sec/pin
- Posted /CAS
- Programmable /CAS Latency: 3, 4, 5, 6
- Write Latency (WL) = Read Latency (RL) - 1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then T<sub>CASE</sub> 85°C, 3.9us at 85°C < T<sub>CASE</sub> ≤ 95°C
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 68 / 60 Ball FBGA – 256Mx4, 8 Banks
- PCB Height: 1.25 inch (30.00mm)
- All of Lead-free products are compliant for RoHS

## ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
256Mx4 (1GB) based module	A0-A13	A0-A9	BA0-BA2	A10



**GR2DR4BD-E4GBXXX**

**DDR2 4GB 2 RANKS ECC REGISTERED DIMM**

**PIN CONFIGURATIONS (Front Side/ Back Side)**

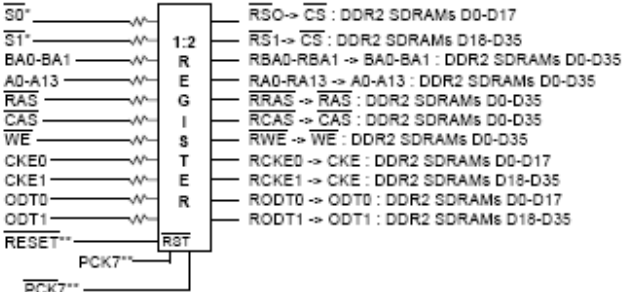
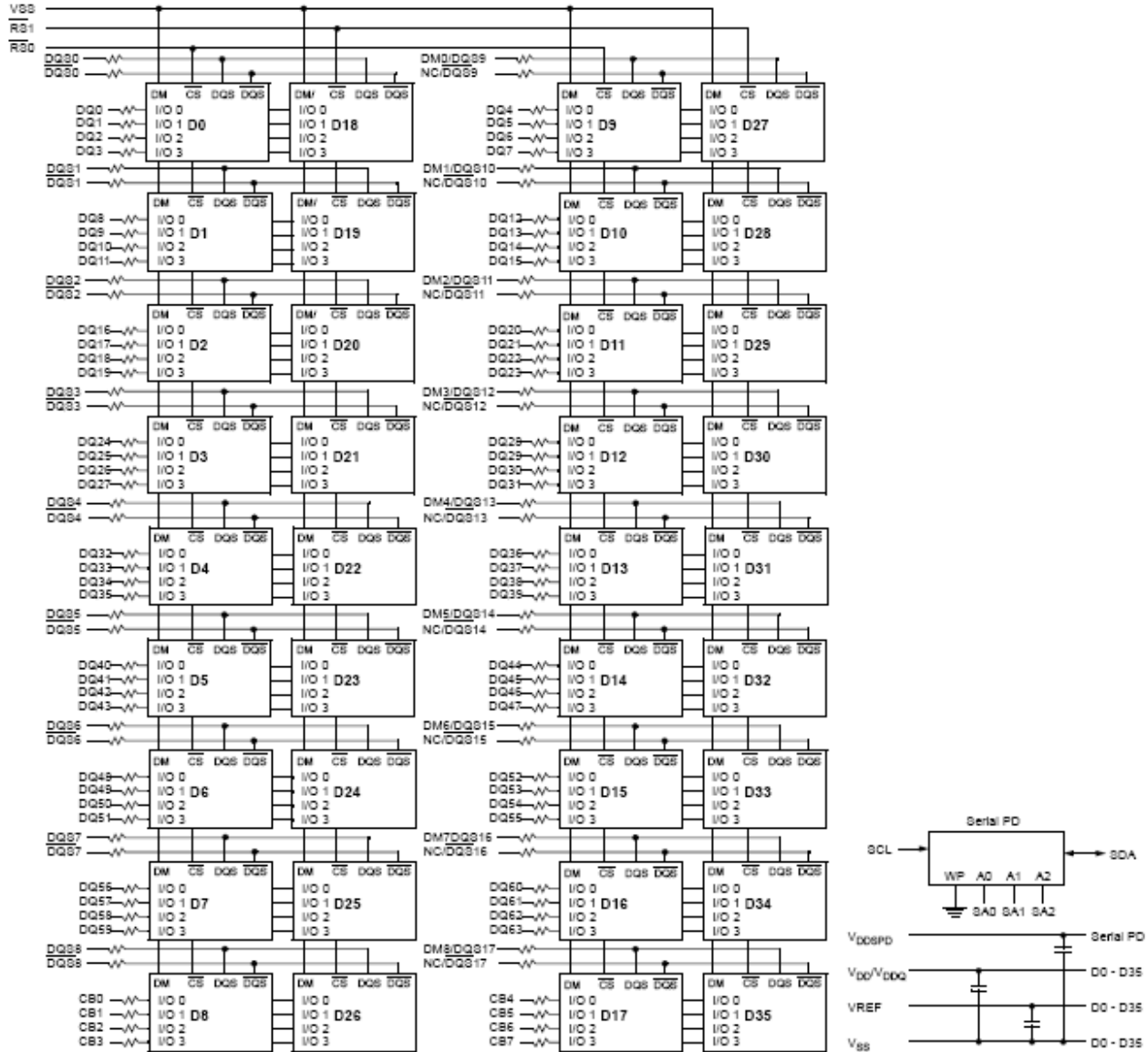
Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK
1	VREF	121	VSS	62	VDDQ	182	A3
2	VSS	122	DQ4	63	A2	183	A1
3	DQ0	123	DQ5	64	VDD	184	VDD
4	DQ1	124	VSS	KEY		KEY	
5	VSS	125	DM0 / DQS9	65	VSS	185	/CK0
6	/DQS0	126	/DQS9	66	VSS	186	CK0
7	DQS0	127	VSS	67	VDD	187	VDD
8	VSS	128	DQ6	68	NC	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDDQ
12	DQ8	132	DQ13	72	VDDQ	192	/RAS
13	DQ9	133	VSS	73	/WE	193	/CS0
14	VSS	134	DM1 / DQS10	74	/CAS	194	VDDQ
15	/DQS1	135	/DQS10	75	VDDQ	195	ODT0
16	DQS1	136	VSS	76	VSS	196	A13
17	VSS	137	NC	77	ODT1	197	VDD
18	/RESET	138	NC	78	VDDQ	198	VSS
19	NC	139	VSS	79	VSS	199	DQ36
20	VSS	140	DQ14	80	DQ32	200	DQ37
21	DQ10	141	DQ15	81	DQ33	201	VSS
22	DQ11	142	VSS	82	VSS	202	DQ38
23	VSS	143	DQ20	83	/DQS4	203	DQ39
24	DQ16	144	DQ21	84	DQS4	204	VSS
25	DQ17	145	VSS	85	VSS	205	DQ38
26	VSS	146	DM2 / DQS11	86	DQ34	206	DQ39
27	/DQS2	147	/DQS11	87	DQ35	207	VSS
28	DQS2	148	VSS	88	VSS	208	DQ44
29	VSS	149	DQ22	89	DQ40	209	DQ45
30	DQ18	150	DQ23	90	DQ41	210	VSS
31	DQ19	151	VSS	91	VSS	211	DM5 / DQS14
32	VSS	152	DQ28	92	/DQS5	212	/DQS14
33	DQ24	153	DQ29	93	DQS5	213	VSS
34	DQ25	154	VSS	94	VSS	214	DQ46
35	VSS	155	DM3 / DQS12	95	DQ42	215	DQ47
36	/DQS3	156	/DQS12	96	DQ43	216	VSS
37	DQS3	157	VSS	97	VSS	217	DQ52
38	VSS	158	DQ30	98	DQ48	218	DQ53
39	DQ26	159	DQ31	99	DQ49	219	VSS
40	DQ27	160	VSS	100	VSS	220	NC
41	VSS	161	CB4	101	SA2	221	NC
42	CB0	162	CB5	102	NC	222	VSS
43	CB1	163	VSS	103	VSS	223	DM6 / DQS15
44	VSS	164	DM8 / DQS17	104	/DQS6	224	/DQS15
45	/DQS8	165	/DQS17	105	DQS6	225	VSS
46	DQS8	166	VSS	106	VSS	226	DQ54
47	VSS	167	CB6	107	DQ50	227	DQ55
48	CB2	168	CB7	108	DQ51	228	VSS
49	CB3	169	VSS	109	VSS	229	DQ60
50	VSS	170	VDDQ	110	DQ56	230	DQ61
51	VDDQ	171	NC / CKE1	111	DQ57	231	VSS
52	CKE0	172	VDD	112	VSS	232	DM7 / DQS16
53	VDD	173	NC	113	/DQS7	233	/DQS16
54	NC	174	NC	114	DQS7	234	VSS
55	NC	175	VDDQ	115	VSS	235	DQ62
56	VDDQ	176	A12	116	DQ58	236	DQ63
57	A11	177	A9	117	DQ59	237	VSS
58	A7	178	VDD	118	VSS	238	VDDSPD
59	VDD	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1
61	A4	181	VDDQ				

## INPUT/OUTPUT FUNCTIONAL DESCRIPTION

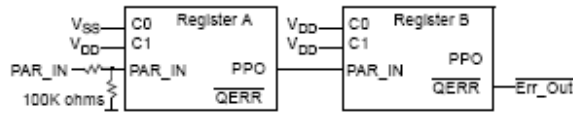
Symbol	Type	Polarity	Function
CK0, /CK0	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and the falling edge of CK*. An on-board DLL circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE [1:0]	Input	Active High	CKE high activates and CKE low deactivates internal signals and device input buffers and output drivers of the SDRAMs. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank).
/CS [1:0]	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both CS*[1:0] are high, all register outputs (except CK, ODT and Chip select) remain in the previous state.
ODT [1:0]	Input	Active High	On-Die Termination control signals
/RAS, /CAS, /WE	Input	Active Low	When sampled at the positive edge of the clock, RAS*, CAS* and WE* define the operation to be executed by the SDRAM.
DM [8:0]	Input	Active High	Masks write data when high, issued concurrently with input data.
BA [2:0]	Input	-	Selects which internal SDRAM memory bank is activated
A [13:0]	Input	-	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10 (=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input/Output pins.
DQS [17:0] /DQS[17:0]	I/O	Cross point	The data strobes, associated with one data byte, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sourced by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS* signals are complements, and timing is relative to the crosspoint of respective DQS and DQS*. If the module is to be operated in single ended strobe mode, all DQS* signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA [2:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
/RESET	Input	-	The /RESET pin is connected to the RST* pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and the register(s) will be set to low level. The PLL will remain synchronized with the input clock.
V <sub>DD</sub> , V <sub>SS</sub>	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V <sub>REF</sub>	Supply	-	Reference voltage for the SSTL-18 inputs.
V <sub>DDSPD</sub>	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.

**DDR2 4GB 2 RANKS ECC REGISTERED DIMM**

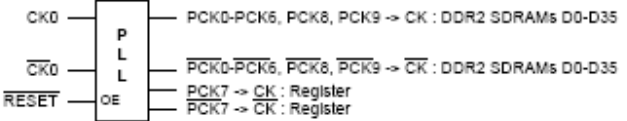
**FUNCTIONAL BLOCK DIAGRAM**



Signals for Address and Command Parity Function (M393T5160CZA)



The resistors on Par\_In, A13, A14, A15, BA2 and the signal line of Err\_Out refer to the section: "Register Options for Unused Address Inputs"



\* S0 connects to DCS and S1 connects to CSR on a pair of Registers, S1 connects to DCS and S0 connects to CSR on another pair of Registers.

\*\* RESET, PCK7 and PCK7 connects to all Registers. Other signals connect to one pair of four Registers.

**ABSOLUTE MAXIMUM DC RATINGS**

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Voltage on any pins relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5	2.3	V
Voltage on $V_{DD}$ relative to $V_{SS}$	$V_{DD}$	-1.0	2.3	V
Voltage on $V_{DDQ}$ relative to $V_{SS}$	$V_{DDQ}$	-0.5	2.3	V
Storage temperature range	$T_{STG}$	-55	+100	°C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**OPERATING TEMPERATURE RANGE**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
DIMM Module Operating Temperature Range (ambient)	$T_{OPR}$	0	+55	°C	
DRAM Component Case Temperature Range	$T_{CASE}$	0	+95	°C	1 - 4

1. DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85 °C DRAM case temperature the Auto-Refresh command interval has to be reduced to  $t_{REF1} = 3.9\mu s$ .
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 °C case temperature before initiating self-refresh operation.

**AC & DC OPERATING CONDITIONS**

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Norm.	Max.		
Device Supply Voltage	$V_{DD}$	1.7	1.8	1.9	V	-
Output Supply Voltage	$V_{DDQ}$	1.7	1.8	1.9	V	1)
Input Reference Voltage	$V_{REF}$	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)
EEPROM Supply Voltage	$V_{DDSPD}$	1.7	-	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	$V_{REF} + 0.125$	-	$V_{DDQ} + 0.3$	V	
DC Input Logic Low	$V_{IL(DC)}$	-0.30	-	$V_{REF} - 0.125$	V	
In/Output Leakage Current	$I_L$	-5	-	5	uA	3)

1. Under all conditions,  $V_{DDQ}$  must be less than or equal to  $V_{DD}$
2. Peak to peak AC noise on  $V_{REF}$  may not exceed  $\pm 2\% V_{REF(DC)}$ .  $V_{REF}$  is also expected to track noise variations in  $V_{DDQ}$ .
3. For any pin on the DIMM connector under test input of  $0 \leq V_{IN} \leq V_{DDQ} + 0.3V$ .

**I<sub>DD</sub> SPECIFICATION**

Symbol	DDR2-800@CL=6	DDR2-667@CL=5	DDR2-533@CL=4	DDR2-400@CL=3	Unit	Note
I <sub>DD0</sub>	4950	1760	1615	1470	mA	2
I <sub>DD1</sub>	2120	1920	1765	1610	mA	2
I <sub>DD2P</sub>	910	850	790	730	mA	3
I <sub>DD2Q</sub>	1520	1430	1340	1160	mA	3
I <sub>DD2N</sub>	1470	1310	1240	1080	mA	3
I <sub>DD3P(F)</sub>	1540	1350	1160	1060	mA	3
I <sub>DD3P(S)</sub>	1024	954	854	754	mA	3
I <sub>DD3N</sub>	1595	1435	1365	1205	mA	3
I <sub>DD4W</sub>	2675	2360	2135	1820	mA	2
I <sub>DD4R</sub>	2905	2480	2145	1855	mA	2
I <sub>DD5B</sub>	2945	2705	2510	2270	mA	3
I <sub>DD6</sub>	270	270	270	270	mA	3
I <sub>DD7</sub>	4180	3795	3455	3070	mA	2

**Notes:**

1. Calculated values from component data. ODT disabled. I<sub>DD1</sub>, I<sub>DD4R</sub>, and I<sub>DD7</sub> are defined with the outputs disabled. Currents includes Registers and PLL.
2. The other rank is in I<sub>DD2P</sub> Precharge Power-Down Standby Current mode
3. Both ranks are in the same I<sub>DD</sub> current mode.

**SPEED BINS & CL, t<sub>RCD</sub>, t<sub>RP</sub>, t<sub>RC</sub> and t<sub>RAS</sub> for CORRESPONDING BIN**

Speed	DDR2-800		DDR2-667		DDR2-533		DDR2-400		Unit
Bin (CL-t <sub>RCD</sub> -t <sub>RP</sub> )	6-6-6		5-5-5		4-4-4		3-3-3		
Parameter	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>CK</sub> , CL=3	-	-	5	8	5	8	5	8	ns
t <sub>CK</sub> , CL=4	3.75	8	3.75	8	3.75	8	5	8	ns
t <sub>CK</sub> , CL=5	3	8	3	8	3.75	8	-	-	ns
t <sub>CK</sub> , CL=6	2.5	8	-	-	-	-	-	-	ns
t <sub>RCD</sub>	15	-	15	-	15	-	15	-	ns
t <sub>RP</sub>	15	-	15	-	15	-	15	-	ns
t <sub>RC</sub>	60	-	60	-	60	-	55	-	ns
t <sub>RAS</sub>	45	70000	45	70000	45	70000	40	70000	ns

**PACKAGE DIMENSION (UNIT: mm)**

