1GB & 2GB DDR2 REGISTERED DIMMs (LOW PROFILE)

GENERAL DESCRIPTION

The Gigaram **GR2DR4B-Exxx/yyy/LP** is a 128M/256M bit x 72 DDDR2 SDRAM high density JEDEC standard ECC Registered memory module. The Gigaram **GR2DR4B-Exxx/yyy/LP** consists of eighteen CMOS 128MX4 DDR2 for 1GB and thirty-six CMOS 128M x 4 DDDR2 SDRAMs for 2GB in 60pin FBGA packages, mounted on a 240PIN glass-epoxy substrate.

DDR2 REGISTERED DIMM PART INFORMATION

Part Number	Density	Organization	Component	Number of Rank	Height
GR2DR4B-E1GB/533/LP	1GB	128MX72	128MX4 * 18	1	0.720 Inch
GR2DR4B-E2GB/533/LP	2GB	256MX72	128MX4 * 36	2	0.720 Inch

Part Number	Density	Organization	Component	Number of Rank	Height
GR2DR4B-E1GB/400/LP	1GB	128MX72	128MX4 * 18	1	0.720 Inch
GR2DR4B-E2GB/400/LP	2GB	256MX72	128MX4 * 36	2	0.720 Inch

FEATURES

- Performance range

Part Number	DDR2-533	DDR2-400
Speed @ CL3	400	400
Speed @ CL4	533	400
CL-tRCD-tRP	4-4-4	3-3-3

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8 ± 0.1V
- 200Mhz f_{CK} for 400Mb/sec/pin, 267Mhz f_{CK} for 533Mb/sec/pin
- 4 Bank
- Posted /CAS
- Programmable /CAS Latency: 3, 4, 5
- Write Latency (WL) = Read Latency (RL) -1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60ball FBGA – 64MX4/128MX4

ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128MX4 (512MB)	A0-A13	A0-A9, A11	BA0-BA1	A10

PIN CONFIGURATIONS (Front Side/ Back Side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	121	V_{SS}	31	DQ19	151	V_{SS}	61	A4	181	V_{DDQ}	91	V_{SS}	211	DQS14
2	V_{SS}	122	DQ4	32	V_{SS}	152	DQ28	62	V_{DDQ}	182	A3	92	/DQS5	212	/DQS14
3	DQ0	123	DQ5	33	DQ24	153	DQ29	63	A2	183	A1	93	DQS5	213	V_{SS}
4	DQ1	124	V_{SS}	34	DQ25	154	V_{SS}	64	V_{DD}	184	V_{DD}	94	V_{SS}	214	DQ46
5	V_{SS}	125	DQS9	35	V_{SS}	155	DQS12					95	DQ42	215	DQ47
6	/DQS0	126	/DQS9	36	/DQS3	156	/DQS12	65	V_{SS}	185	CK0	96	DQ43	216	V_{SS}
7	DQS0	127	V_{SS}	37	DQS3	157	V_{SS}	66	V_{SS}	186	/CK0	97	V_{SS}	217	DQ52
8	V_{SS}	128	DQ6	38	V_{SS}	158	DQ30	67	V_{DD}	187	V_{DD}	98	DQ48	218	DQ53
9	DQ2	129	DQ7	39	DQ26	159	DQ31	68	Par_In	188	A0	99	DQ49	219	V_{SS}
10	DQ3	130	V_{SS}	40	DQ27	160	V_{SS}	69	V_{DD}	189	V_{DD}	100	V_{SS}	220	RFU
11	V_{SS}	131	DQ12	41	V_{SS}	161	CB4	70	A10	190	BA1	101	SA2	221	RFU
12	DQ8	132	DQ13	42	CB0	162	CB5	71	BA0	191	V_{DDQ}	102	NC	222	V_{SS}
13	DQ9	133	V_{SS}	43	CB1	163	V_{SS}	72	V_{DDQ}	192	/RAS	103	V_{SS}	223	DQS15
14	V_{SS}	134	DQS10	44	V_{SS}	164	DQS17	73	/WE	193	/S0	104	/DQS6	224	/DQS15
15	/DQS1	135	/DQS10	45	/DQS8	165	/DQS17	74	/CAS	194	V_{DDQ}	105	DQW6	225	V_{SS}
16	DQS1	136	V_{SS}	46	DQS8	166	V_{SS}	75	V_{DDQ}	195	ODT0	106	V_{SS}	226	DQ54
17	V_{SS}	137	RFU	47	V_{SS}	167	CB6	76	/S1	196	A13	107	DQ50	227	DQ55
18	/RESET	138	RFU	48	CB2	168	CB7	77	ODT1	197	V_{DD}	108	DQ51	228	V_{SS}
19	NC	139	V_{SS}	49	CB3	169	V_{SS}	78	V_{DDQ}	198	V_{SS}	109	V_{SS}	229	DQ60
20	V_{SS}	140	DQ14	50	V_{SS}	170	V_{DDQ}	79	V_{SS}	199	DQ36	110	DQ56	230	DQ61
21	DQ10	141	DQ15	51	V_{DDQ}	171	CKE1	80	DQ32	200	DQ37	111	DQ57	231	V_{SS}
22	DQ11	142	V_{SS}	52	CKE0	172	V_{DD}	81	DQ33	201	V_{SS}	112	V_{SS}	232	DQS16
23	V_{SS}	143	DQ20	53	V_{DD}	173	NC	82	V_{SS}	202	DQS13	113	/DQS7	233	/DQS16
24	DQ16	144	DQ21	54	NC	174	NC	83	/DQS4	203	/DQS13	114	DQS7	234	V_{SS}
25	DQ17	145	V_{SS}	55	/Err-Out	175	V_{DDQ}	84	DQS4	204	V_{SS}	115	V_{SS}	235	DQ62
26	V_{SS}	146	DQS11	56	V_{DDQ}	176	A12	85	V_{SS}	205	DQ38	116	DQ58	236	DQ63
27	/DQS2	147	/DQS11	57	A11	177	A9	86	DQ34	206	DQ39	117	DQ59	237	V_{SS}
28	DQS2	148	V_{SS}	58	A7	178	V_{DD}	87	DQ35	207	V_{SS}	118	V_{SS}	238	VDDSPD
29	V_{SS}	149	DQ22	59	V_{DD}	179	A8	88	V_{SS}	208	DQ44	119	SDA	239	SA0
30	DQ18	150	DQ23	60	A5	180	A6	89	DQ40	209	DQ45	120	SCL	240	SA1
								90	DQ41	210	V_{SS}				

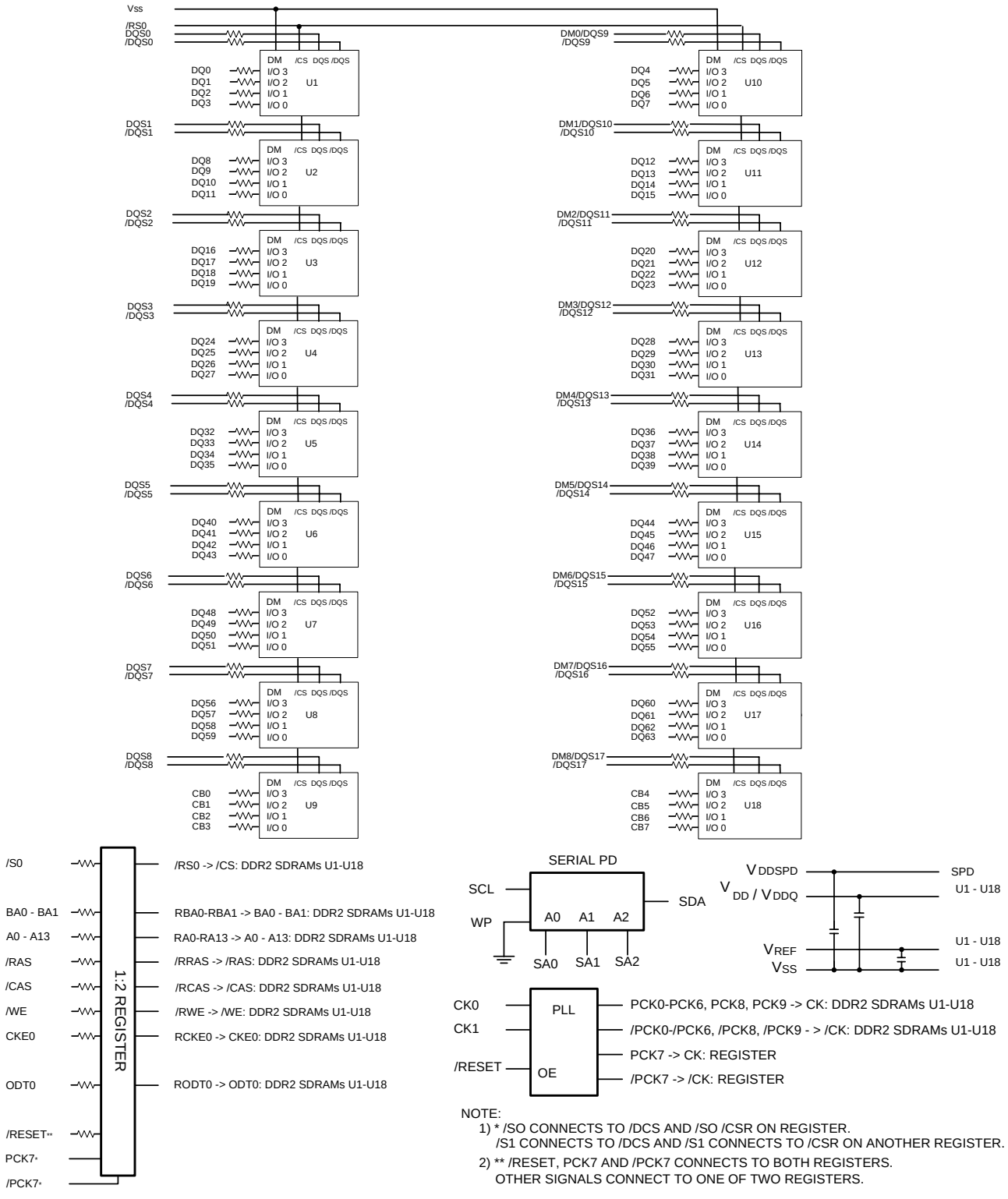
PIN DESCRIPTION

PIN NAME	DESCRIPTION	PIN NAME	DESCRIPTION
CK0	Clock Inputs, positive line	ODT0-ODT1	On die Termination
/CK0	Clock Inputs, negative line	DQ0-DQ63	Data Input/Output
CKE0, CKE1	Clock Enables	CB0-CB7	Data checks bits Input/Output
/RAS	Row Address Strobe	DQS0-DQS8	Data Strobes
/CAS	Column Address Strobe	/DQS0-/DQS8	Data strobes, negative line
/WE	Write Enables	DM(0-8), DQS(9-17)	Data Masks / Data Strobes (Read)
/S0, /S1	Chip Selects	/DQS9-/DQS17	Data Strobes (Read), negative line
A0-A9, A11-A13	Address Inputs	RFU	Reserved for Future Use
A10/AP	Address Inputs/Autoprecharge	NC	No Connect
BA0, BA1	DDR2 SDRAM Bank Address	TEST	Memory bus test tool
SCL	SPD Clock Input	V_{DD}	Core Power
SDA	SPD Data Input/Output	V_{DDQ}	I/O Power
SA0-SA2	SPD Address	V_{SS}	Ground
Par_In	Parity bit for the Address and Control Bus	V_{REF}	Input/Output Reference
/Err_Out	Parity error found in the Address& Control Bus	V_{DDSPD}	SPD Power
/RESET	Registered and PLL control Pin		

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

SYMBOL	TYPE	FUNCTION
CK0	Input	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL
/CK0	Input	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE0-CKE1	Input	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down Mode, or the Self Refresh mode.
/S0-/S1	Input	Enables the associated SDRAM command decoder when low and disable decoder when high. When decoder is disabled, new commands are ignored but previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the registers on the DIMM when both inputs are high.
ODT0-ODT1	Input	I/O bus impedance control signals.
/RAS, /CAS, /WE	Input	When sampled at the positive rising edge of the clock, /CAS, /RAS and /WE define the operation to be executed by the SDRAM.
V_{REF}	Supply	Reference voltage for SSTL_18 inputs.
V_{DDQ}	Supply	Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity.
BA0-BA1	Input	Selects which SDRAM bank of four is activated.
A0-A9, A10/AP, A11-A13	Input	During a Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0-DQ63, CB0-CB7	In/Out	Data and Check Bit Input/Output pins
DM0-DM8	Input	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
V_{DD}, V_{SS}	Supply	Power and ground for the DDR SDRAM input buffers and core logic.
DQS0-DQS17	In/Out	Positive line of the differential data strobe for input and output data.
/DQS0-/DQS17	In/Out	Negative line of the differential data strobe for input and output data.
SA0-SA2	Input	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	In/Out	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} to act as a pullup.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A register may be connected from the SCL bus time to V_{DDSPD} to act as a pullup.
V_{DDSPD}	Supply	Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports from 1.7 volt to 3.6 vold operation).
/RESET	Input	The /RESET pin is connected to the /RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (The PLL will be remain synchronized with the input clock)
Par_In	Input	Parity bit for the Address and Control bus ("1": Odd, "0":Even)
/Err_Out	Input	Parity error found in the Address and Control bus.
TEST	In/Out	Used by memory bus analysis tools (unused on memory DIMMs)

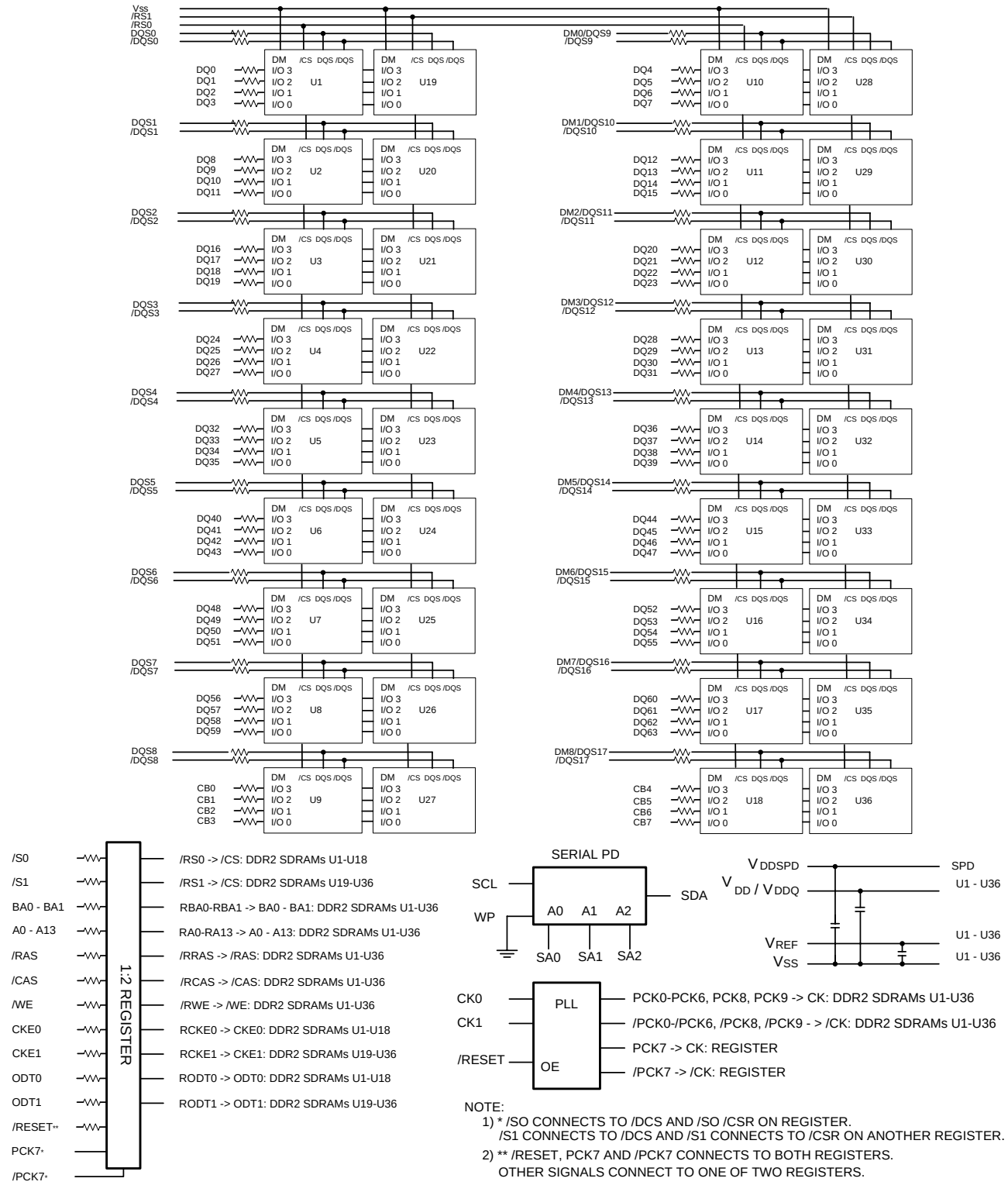
FUNCTIONAL BLOCK DIAGRAM: 1GB, 128MX72 MODULE USING 128MX4 (GR2DR4B-E1GB/LP)



NOTE:

1) * /SO CONNECTS TO /DCS AND /SO /CSR ON REGISTER.
   /S1 CONNECTS TO /DCS AND /S1 CONNECTS TO /CSR ON ANOTHER REGISTER.
2) ** /RESET, PCK7 AND /PCK7 CONNECTS TO BOTH REGISTERS.
   OTHER SIGNALS CONNECT TO ONE OF TWO REGISTERS.

FUNCTIONAL BLOCK DIAGRAM: 2GB, 256MX72 MODULE USING 128MX4 (GR2DR4B-E2GB/LP)



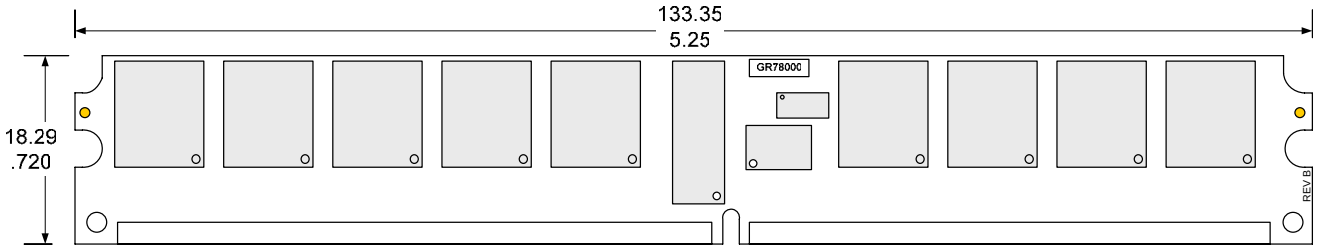
NOTE:

1) * /SO CONNECTS TO /DCS AND /SO /CSR ON REGISTER.
/S1 CONNECTS TO /DCS AND /S1 CONNECTS TO /CSR ON ANOTHER REGISTER.

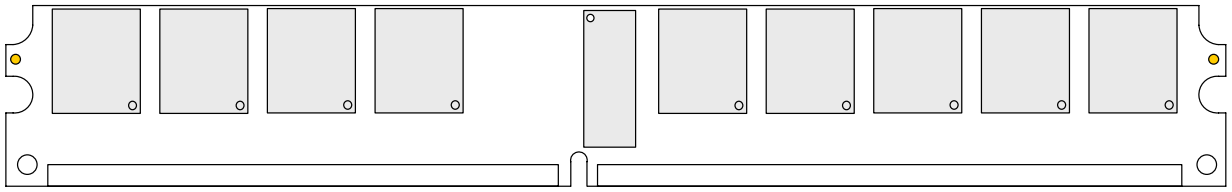
2) ** /RESET, PCK7 AND /PCK7 CONNECTS TO BOTH REGISTERS.
OTHER SIGNALS CONNECT TO ONE OF TWO REGISTERS.

PACKAGE DIMENSIONS (Unit: mm/inch)

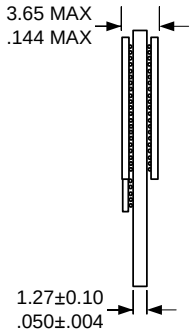
FRONT



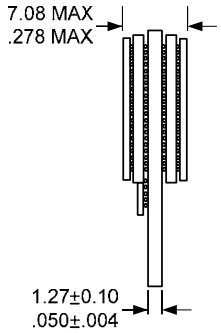
BACK



SIDE



1GB MODULE



2GB MODULE