GENERAL DESCRIPTION

The Gigaram **GR2DR4B-E1GBXXXVLP** is a 128M bit x 72 DDDR2 SDRAM high density ECC REGISTERED DIMM. The **GR2DR4B-E1GBXXXVLP** consists of eighteen CMOS 128M x 4 DDR2 SDRAMs for 1GB in 68pin FBGA packages, mounted on a 240PIN glass-epoxy substrate.

DDR2 ECC REGISTERED DIMM PART INFORMATION

Part Number	Density	Organization	Component	Rank	Height
GR2DR4B-E1GB667VLP	1GB	128MX72	128Mx4 * 18	1	0.72 Inch
GR2DR4B-E1GB533VLP	1GB	128MX72	128Mx4 * 18	1	0.72 Inch
GR2DR4B-E1GB400VLP	1GB	128MX72	128Mx4 * 18	1	0.72 Inch

FEATURES

- Performance range

Part Number	DDR2-667	DDR2-533	DDR2-400
Speed @ CL3	400	400	400
Speed @ CL4	533	533	400
Speed @ CL5	667	533	-
CL-tRCD-tRP	5-5-5	4-4-4	3-3-3

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8 ± 0.1V
- 200Mhz f_{CK} for 400Mb/sec/pin, 267Mhz f_{CK} for 533Mb/sec/pin, 333Mhz f_{CK} for 667Mb/sec/pin
- Posted /CAS
- Programmable /CAS Latency: 3, 4, 5
- Write Latency (WL) = Read Latency (RL) -1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95°C
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 68ball FBGA – 128MX4

ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx4 (512MB) based module	A0-A13	A0-A9	BA0-BA2	A10

PIN CONFIGURATIONS (Front Side/ Back Side)

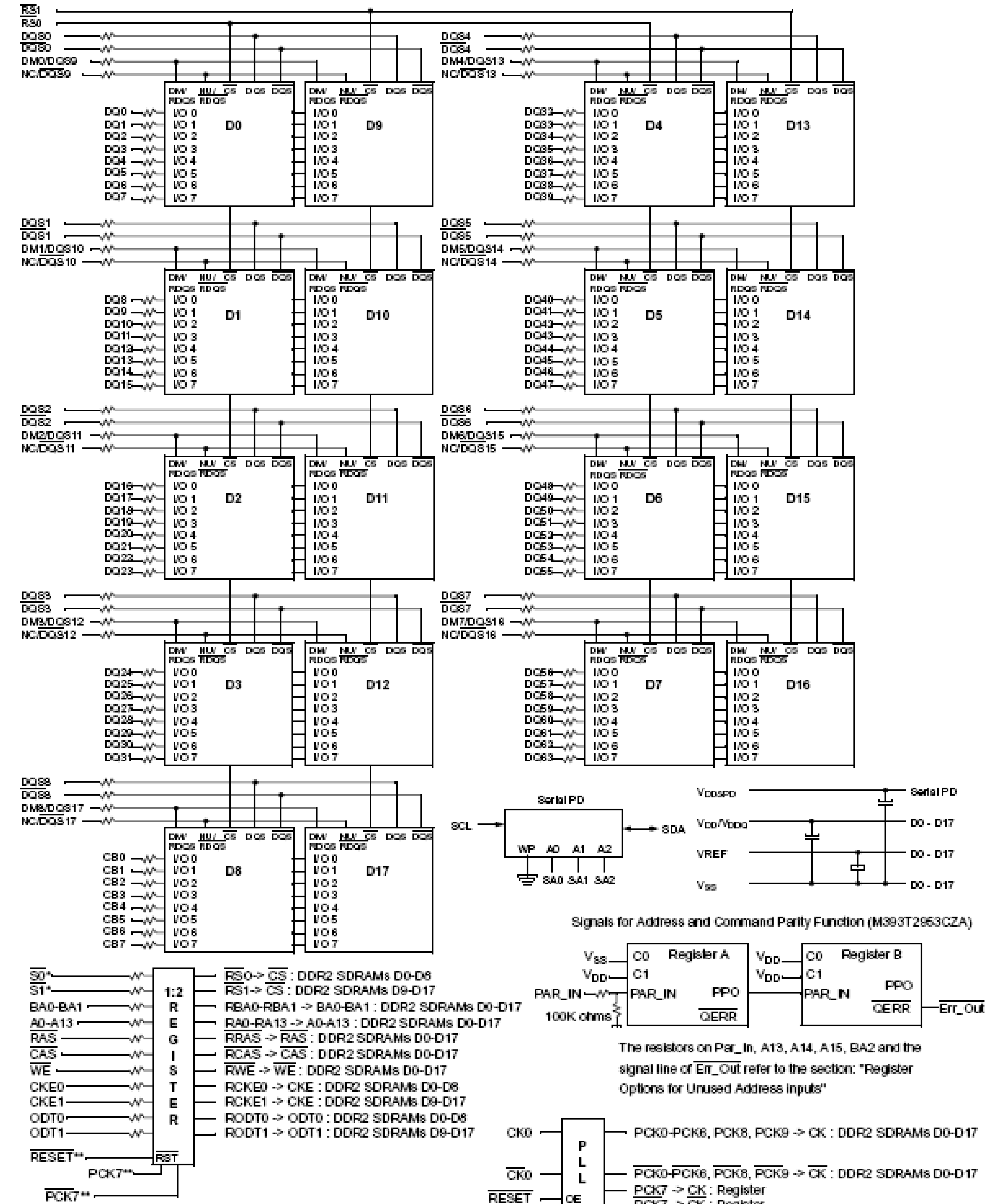
Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK
1	VREF	121	VSS	62	VDDQ	182	A3
2	VSS	122	DQ4	63	A2	183	A1
3	DQ0	123	DQ5	64	VDD	184	VDD
4	DQ1	124	VSS	KEY		KEY	
5	VSS	125	DM0, DQS9	65	VSS	185	CKO*
6	DQS0*	126	DQS9*	66	VSS	186	CK0
7	DQS0	127	VSS	67	VDD	187	VDD
8	VSS	128	DQ6	68	NC	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDDQ
12	DQ8	132	DQ13	72	VDDQ	192	RAS*
13	DQ9	133	VSS	73	WE*	193	CS0*
14	VSS	134	DM1, DQS10	74	CAS*	194	VDDQ
15	DQS1*	135	DQS10*	75	VDDQ	195	ODT0
16	DQS1	136	VSS	76	VSS	196	A13
17	VSS	137	NC	77	ODT1	197	VDD
18	RESET*	138	NC	78	VDDQ	198	VSS
19	NC	139	VSS*	79	VSS	199	DQ36
20	VSS	140	DQ14	80	DQ32	200	DQ37
21	DQ10	141	DQ15	81	DQ33	201	VSS
22	DQ11	142	VSS	82	VSS	202	DQ38
23	VSS	143	DQ20	83	DQS4*	203	DQ39
24	DQ16	144	DQ21	84	DQS4	204	VSS
25	DQ17	145	VSS	85	VSS	205	DQ38
26	VSS	146	DM2, DQS11	86	DQ34	206	DQ39
27	DQS2*	147	DQS11*	87	DQ35	207	VSS
28	DQS2	148	VSS	88	VSS	208	DQ44
29	VSS	149	DQ22	89	DQ40	209	DQ45
30	DQ18	150	DQ23	90	DQ41	210	VSS
31	DQ19	151	VSS	91	VSS	211	DM5, DQS14
32	VSS	152	DQ28	92	DQS5*	212	DQS14*
33	DQ24	153	DQ29	93	DQS5	213	VSS
34	DQ25	154	VSS	94	VSS	214	DQ46
35	VSS	155	DM3, DQS12	95	DQ42	215	DQ47
36	DQS3*	156	DQS12*	96	DQ43	216	VSS
37	DQS3	157	VSS	97	VSS	217	DQ52
38	VSS	158	DQ30	98	DQ48	218	DQ53
39	DQ26	159	DQ31	99	DQ49	219	VSS
40	DQ27	160	VSS	100	VSS	220	NC
41	VSS	161	CB4	101	SA2	221	NC
42	CB0	162	CB5	102	NC	222	VSS
43	CB1	163	VSS	103	VSS	223	DM6, DQS15
44	VSS	164	DM8, DQS17	104	DQS6*	224	DQS15*
45	DQS8*	165	DQS17*	105	DQS6	225	VSS
46	DQS8	166	VSS	106	VSS	226	DQ54
47	VSS	167	CB6	107	DQ50	227	DQ55
48	CB2	168	CB7	108	DQ51	228	VSS
49	CB3	169	VSS	109	VSS	229	DQ60
50	VSS	170	VDDQ	110	DQ56	230	DQ61
51	VDDQ	171	NC, CKE1	111	DQ57	231	VSS
52	CKE0	172	VDD	112	VSS	232	DM7, DQS16
53	VDD	173	NC	113	DQS7*	233	DQS16*
54	NC	174	NC	114	DQS7	234	VSS
55	NC	175	VDDQ	115	VSS	235	DQ62
56	VDDQ	176	A12	116	DQ58	236	DQ63
57	A11	177	A9	117	DQ59	237	VSS
58	A7	178	VDD	118	VSS	238	VDDSPD
59	VDD	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1
61	A4	181	VDDQ				

REGISTERED DIMM INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Polarity	Function
CK0, /CK0	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and he falling edge of CK*. An on-board DLL circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE [1:0]	Input	Active High	CKE high activates and CKE low deactivates internal signals and device input buffers and output drivers of the SDRAMs. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank).
/CS [1:0]	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both CS*[1:0] are high, all register outputs (except CK, ODT and Chip select) remain in the previous state.
ODT [1:0]	Input	Active High	On-Die Termination control signals
/RAS, /CAS, /WE	Input	Active Low	When sampled at the positive edge of the clock, RAS*, CAS* and WE* define the operation to be executed by the SDRAM.
DM [8:0]	Input	Active High	Masks write data when high, issued concurrently with input data.
BA [2:0]	Input	-	Selects which internal SDRAM memory bank is activated
A [13:0]	Input	-	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10 (=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input/Output pins.
DQS [17:0] /DQS[17:0]	I/O	Cross point	The data strobes, associated with one data byte, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sources by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS* signals are complements, and timing is relative to the crosspoint of respective DQS and DQS*. If the module is to be operated in single ended strobe mode, all DQS* signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA [2:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
RESET*	Input	-	The RESET* pin is connected to the RST* pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and the register(s) will be set to low level. The PLL will remain synchronized with the input clock.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V_{REF}	Supply	-	Reference voltage for the SSTL-18 inputs.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.

Note: /CS1, ODT1 and CKE1 are used on dual rank modules only.

FUNCTIONAL BLOCK DIAGRAM



* S0 connects to DCS and S1 connects to CSR on a Register,
S1 connects to DCS and S0 connects to CSR on another Register.

** RESET, PCK7 and PCK7 connects to both Registers.
Other signals connect to one of two Registers.

Notes :
1. DQ-to-I/O wiring may be changed per nibble.
2. Unless otherwise noted, resister values are 22 Ohms
3. RS0 and RS1 alternate between the back and front sides of the DIMM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	2.3	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0	2.3	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5	2.3	V
Storage temperature range	T_{STG}	-55	+100	° C

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING TEMPERATURE RANGE

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
DIMM Module Operating Temperature Range (ambient)	TOPR	0	+55	° C	
DRAM Component Case Temperature Range	TCASE	0	+95	° C	1 - 4

1. DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85 ° C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREF1= 3.9us.
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 ° C case temperature before initiating self-refresh operation.

SUPPLY VOLTAGE LEVELS AND DC OPERATING CONDITIONS

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Norm.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
EEPROM Supply Voltage	V_{DDSPD}	1.7	-	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	-	V_{DDQ} + 0.3	V	
DC Input Logic Low	$V_{IL(DC)}$	-0.30	-	V_{REF} – 0.125	V	
In/Output Leakage Current	I_L	-5	-	5	uA	3)

1. Under all conditions, V_{DDQ} must be less than or equal to VDD
2. Peak to peak AC noise on V_{REF} may not exceed $\pm$ 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
3. For any pin on the DIMM connector under test input of 0 V$\leq$ V_{IN} $\leq$ V_{DDQ} + 0.3V.

I_{DD} SPECIFICATION

Symbol	DDR2-667@CL=5	DDR2-533@CL=4.	DDR2-400@CL=3	Unit	Note
I_{DD0}	1,960	3,170	3,040	mA	1, 2
I_{DD1}	2,220	3,420	3,370	mA	1, 2
I_{DD2P}	780	1,480	1,380	mA	1, 2
I_{DD2N}	2,400	2,360	2,210	mA	1, 2
I_{DD2Q}	2,040	2,600	2,320	mA	1, 2
$I_{DD3P(F)}$	1,280	2,240	2,140	mA	1, 2
$I_{DD3P(S)}$	810	1,138	1,088	mA	1, 2
I_{DD3N}	2,400	2,590	2,330	mA	1, 2
I_{DD4R}	3,030	3,770	3,260	mA	1, 2
I_{DD4W}	3,210	3,920	3,360	mA	1, 2
I_{DD5B}	3,210	5,550	5,230	mA	1, 2
I_{DD6}	180	540	540	mA	1, 2
I_{DD7}	3,330	7,610	6,630	mA	1, 2

Notes:
1. Calculated values from component data. ODT disabled. IDD1, IDD4R, and IDD7 are defined with the outputs disabled. Currents includes Registers and PLL.
2. The other rank is in IDD2P Precharge Power-Down Standby Current mode
3. Both ranks are in the same IDD current mode.

PACKAGE DIMENSION (UNIT: mm)