GENERAL DESCRIPTION

The Gigaram **GR2DM8B-E1GBXXX** DDR2 SDRAM module is high speed, CMOS, dynamic random-access 1GB memory module organized in x72 configuration. This module use internally configured eight-bank DDR2 128MX8 SDRAM devices.

DDR2 MINI RDIMM PART INFORMATION

Part Number	Density	Organization	Component	Rank	Height
GR2DM8B-E1GB800	1GB	128MX72	128Mx8 * 9	1	1.25 Inch
GR2DM8B-E1GB667	1GB	128MX72	128Mx8 * 9	1	1.25 Inch
GR2DM8B-E1GB533	1GB	128MX72	128Mx8 * 9	1	1.25 Inch
GR2DM8B-E1GB400	1GB	128MX72	128Mx8 * 9	1	1.25 Inch

FEATURES

- Performance range

Part Number	DDR2-800	DDR2-667	DDR2-533	DDR2-400	Unit
Speed @ CL3	400	400	400	400	Mbps
Speed @ CL4	533	533	533	400	Mbps
Speed @ CL5	800	667	533	-	Mbps
CL-tRCD-tRP	5-5-5	5-5-5	4-4-4	3-3-3	CK

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8 ± 0.1V
- 200Mhz f_{CK} for 400Mb, 267Mhz f_{CK} for 533Mb, 333Mhz f_{CK} for 667Mb/sec/pin, 400Mhz f_{CK} for 800Mb/sec/pin
- Posted /CAS
- Programmable /CAS Latency: 3, 4, 5
- Write Latency (WL) = Read Latency (RL) -1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 92ball FBGA – 128Mx8
- PCB Height: 1.25 inch (30.0mm)
- 244-Pin, Mini dual in-line memory module (MiniDIMM)
- Supports ECC error detection and correction
- All of Lead-free products are compliant for RoHS

ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
128Mx8 (1GB) based module	A0-A13	A0-A9	BA0-BA2	A10

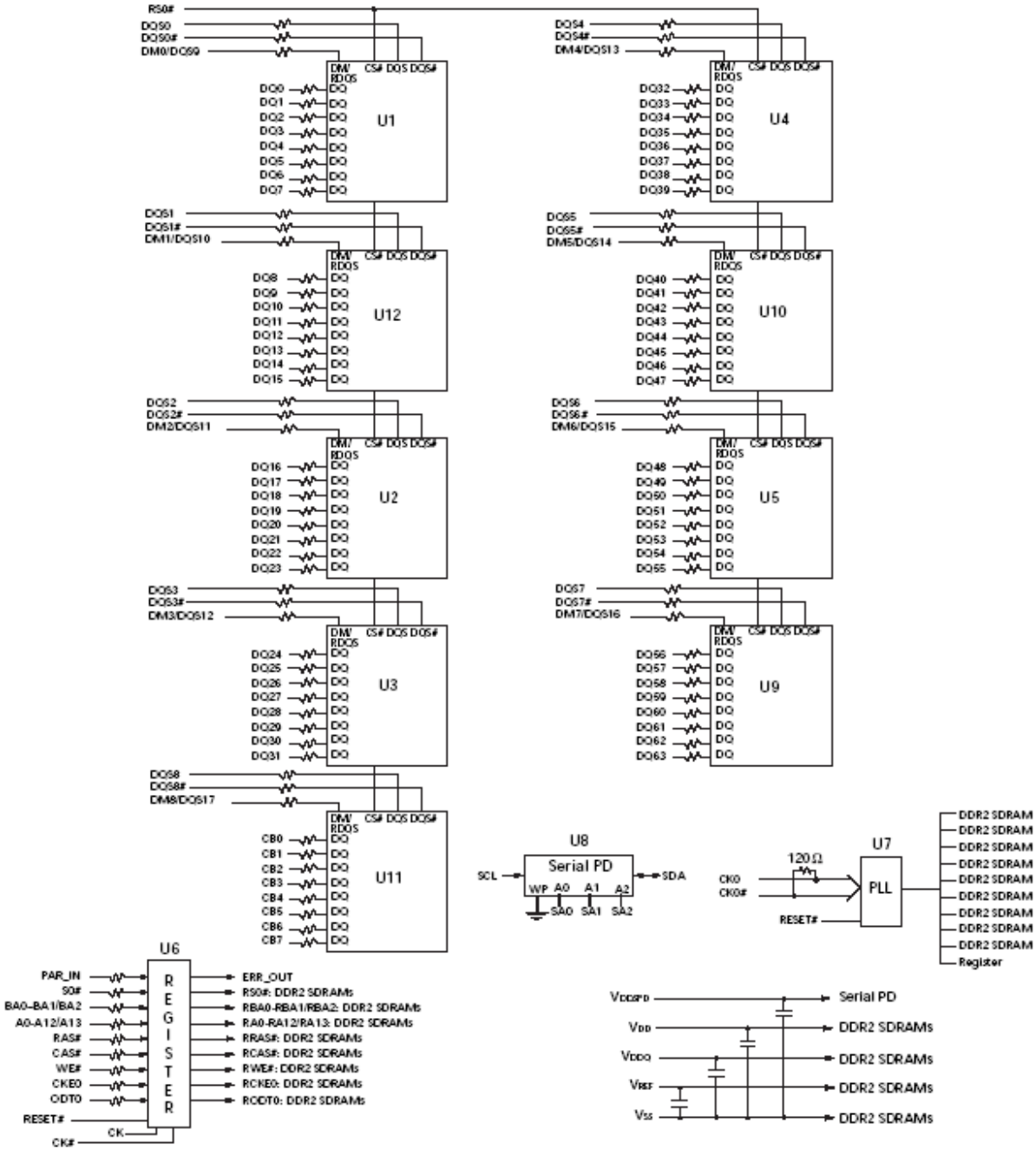
PIN CONFIGURATIONS (Front Side/ Back Side)

Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK
1	VREF	123	VSS	62	A4	184	VDDQ
2	VSS	124	DQ4	63	VDDQ	185	A3
3	DQ0	125	DQ5	64	A2	186	A1
4	DQ1	126	VSS	65	VDD	187	VDD
5	VSS	127	DM0 / RDQS0	66	VSS	188	CK0
6	/DQS0	128	NC / /RDQS0	67	VSS	189	/CK0
7	DQS0	129	VSS	68	PAR_IN	190	VDD
8	VSS	130	DQ6	69	VDD	191	A0
9	DQ2	131	DQ7	70	A10/AP	192	BA1
10	DQ3	132	VSS	71	BA0	193	VDD
11	VSS	133	DQ12	72	VDD	194	/RAS
12	DQ8	134	DQ13	73	/WE	195	VDDQ
13	DQ9	135	VSS	74	VDDQ	196	/CS0
14	VSS	136	DM1/ RDQS1	75	/CAS	197	VDDQ
15	/DQS1	137	NC / /RDQS1	76	VDDQ	198	ODT0
16	DQS1	138	VSS	77	NC	199	A13
17	VSS	139	RFU	78	NC	200	VDD
18	/RESET	140	RFU	79	VDDQ	201	NC
19	NC	141	VSS	80	NC	202	VSS
20	VSS	142	DQ14	81	VSS	203	DQ36
21	DQ10	143	DQ15	82	DQ32	204	DQ37
22	DQ11	144	VSS	83	DQ33	205	VSS
23	VSS	145	DQ20	84	VSS	206	DM4 / RDQS4
24	DQ16	146	DQ21	85	/DQS4	207	NC / /RDQS4
25	DQ17	147	VSS	86	DQS4	208	VSS
26	VSS	148	DM2 / RDQS2	87	VSS	209	DQ38
27	/DQS2	149	NC / /RDQS2	88	DQ34	210	DQ39
28	DQS2	150	VSS	89	DQ35	211	VSS
29	VSS	151	DQ22	90	VSS	212	DQ44
30	DQ18	152	DQ23	91	DQ40	213	DQ45
31	DQ19	153	VSS	92	DQ41	214	VSS
32	VSS	154	DQ28	93	VSS	215	DM5 / RDQS5
33	DQ24	155	DQ29	94	/DQS5	216	NC / /RDQS5
34	DQ25	156	VSS	95	DQS5	217	VSS
35	VSS	157	DM3 / RDQS3	96	VSS	218	DQ46
36	/DQS3	158	NC / /RDQS3	97	DQ42	219	DQ47
37	DQS3	159	VSS	98	DQ43	220	VSS
38	VSS	160	DQ30	99	VSS	221	DQ52
39	DQ26	161	DQ31	100	DQ48	222	DQ53
40	DQ27	162	VSS	101	DQ49	223	VSS
41	VSS	163	CB4	102	VSS	224	RFU
42	CB0	164	CB5	103	SA2	225	RFU
43	CB1	165	VSS	104	NC (TEST)	226	VSS
44	VSS	166	DM8 / RDQS8	105	VSS	227	DM6 / RDQS6
45	/DQS8	167	NC / /RDQS8	106	/DQS6	228	NC / /RDQS6
46	DQS8	168	VSS	107	DQS6	229	VSS
47	VSS	169	CB6	108	VSS	230	DQ54
48	CB2	170	CB7	109	DQ50	231	DQ55
49	CB3	171	VSS	110	DQ51	232	VSS
50	VSS	172	NC	111	VSS	233	DQ60
51	NC	173	VDDQ	112	DQ56	234	DQ61
52	VDDQ	174	NC / CKE1	113	DQ57	235	VSS
53	CKE0	175	VDD	114	VSS	236	DM7 / RDQS7
54	VDD	176	NC	115	/DQS7	237	NC / /RDQS7
55	NC/BA2	177	NC	116	DQS7	238	VSS
56	ERR_OUT	178	VDDQ	117	VSS	239	DQ62
57	VDDQ	179	A12	118	DQ58	240	DQ63
58	A11	180	A9	119	DQ59	241	VSS
59	A7	181	VDD	120	VSS	242	SDA
60	VDD	182	A8	121	SA0	243	SCL
61	A5	183	A6	122	SA1	244	VDDSPD

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Polarity	Function
CK0, /CK0	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and he falling edge of CK*. An on-board DLL circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0	Input	Active High	CKE high activates and CKE low deactivates internal signals and device input buffers and output drivers of the SDRAMs. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank).
/CS0	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue.
ODT0	Input	Active High	On-Die Termination control signals
/RAS, /CAS, /WE	Input	Active Low	When sampled at the positive edge of the clock, RAS*, CAS* and WE* define the operation to be executed by the SDRAM.
DM [8:0]	Input	Active High	Masks write data when high, issued concurrently with input data.
BA [2:0]	Input	-	Selects which internal SDRAM memory bank is activated
A [13:0]	Input	-	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10 (=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ [63:0], CB [7:0]	I/O	-	Data and Check Bit Input/Output pins.
DQS [8:0] /RDQS[8:0]	I/O	Cross point	The data strobes, associated with one data byte, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sources by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS* signals are complements, and timing is relative to the crosspoint of respective DQS and DQS*. If the module is to be operated in single ended strobe mode, all DQS* signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA [2:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
/RESET	Input	-	The /RESET pin is connected to the RST* pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and the register(s) will be set to low level. The PLL will remain synchronized with the input clock.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V_{REF}	Supply	-	Reference voltage for the SSTL-18 inputs.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.

FUNCTIONAL BLOCK DIAGRAM



Notes: 1. Unless otherwise noted, resistor values are 22Ω.

ABSOLUTE MAXIMUM DC RATINGS

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	2.3	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0	2.3	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5	2.3	V
Storage temperature range	T_{STG}	-55	+100	° C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING TEMPERATURE RANGE

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
DIMM Module Operating Temperature Range (ambient)	T_{OPR}	0	+55	° C	
DRAM Component Case Temperature Range	T_{CASE}	0	+85	° C	1 - 4

1. DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85 ° C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREF1= 3.9us.
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 ° C case temperature before initiating self-refresh operation.

SUPPLY VOLTAGE LEVELS AND DC OPERATING CONDITIONS

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Norm.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	V	2)
EEPROM Supply Voltage	V_{DDSPD}	1.7	-	3.6	V	
DC Input Logic High	$V_{IH(DC)}$	V_{REF} + 0.125	-	V_{DDQ} + 0.25	V	
DC Input Logic Low	$V_{IL(DC)}$	0	-	V_{REF} - 0.125	V	
In/Output Leakage Current	I_{LI}	0.10	-	3	uA	3)

1. Under all conditions, V_{DDQ} must be less than or equal to VDD
2. Peak to peak AC noise on V_{REF} may not exceed $\pm$ 2% $V_{REF\,(DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
3. For any pin on the DIMM connector under test input of 0 V$\leq$ V_{IN} $\leq$ V_{DDQ} + 0.3V.

I_{DD} SPECIFICATION

Symbol	DDR2-800@CL=5	DDR2-667@CL=5	DDR2-533@CL=4	DDR2-400@CL=3	Unit	Note
I_{DD0}	810	765	630	630	mA	2
I_{DD1}	990	900	855	810	mA	2
I_{DD2P}	63	63	63	63	mA	3
I_{DD2N}	450	360	360	315	mA	3
I_{DD2Q}	450	360	360	315	mA	3
$I_{DD3P(F)}$	360	270	270	270	mA	3
$I_{DD3P(S)}$	90	90	90	90	mA	3
I_{DD3N}	540	495	405	360	mA	3
I_{DD4W}	1440	1215	1125	945	mA	2
I_{DD4R}	1440	1215	1125	945	mA	2
I_{DD5}	2115	1935	1890	1845	mA	3
I_{DD6}	63	63	63	63	mA	3
I_{DD7}	3015	2520	2430	2340	mA	2

Notes:
1. Calculated values from component data. ODT disabled. I_{DD1}, I_{DD4R}, and I_{DD7} are defined with the outputs disabled. Currents includes Registers and PLL.
2. The other rank is in I_{DD2P} Precharge Power-Down Standby Current mode
3. Both ranks are in the same IDD current mode.

I_{DD} MEASUREMENT TEST CONDITIONS

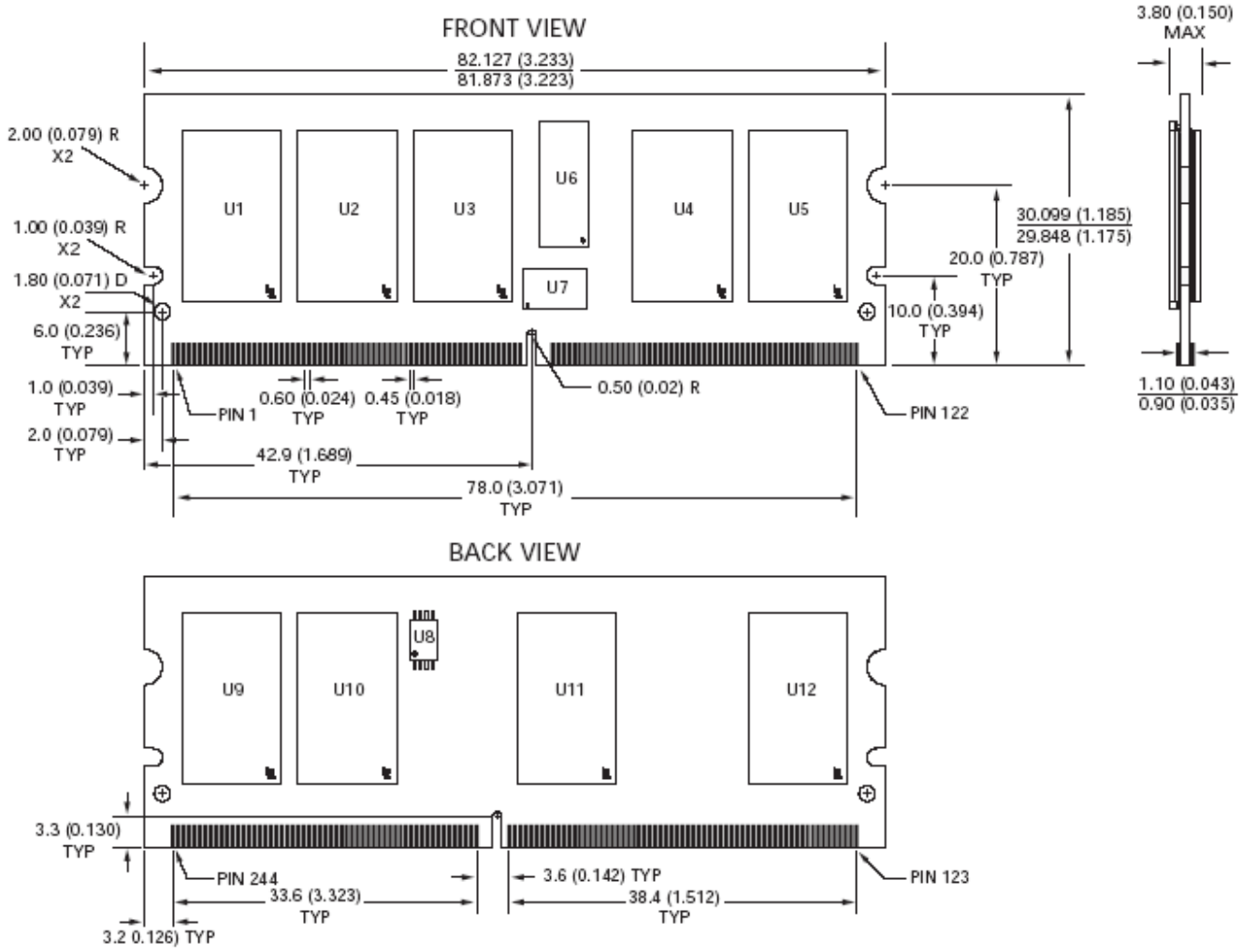
Parameter	Symbol	DDR2-667	Unit
CAS Latency	$CL_{(IDD)}$	5	t_{CK}
Clock Cycle Time	$t_{CK(IDD)}$	3.75	ns
Active to Read or Write delay	$t_{RCD(IDD)}$	15	ns
Active to Active / Auto-Refresh command period	$t_{RC(IDD)}$	60	ns
Active bank A to Active bank B command delay	$t_{RRD(IDD)}$	7.5	ns
Active to Precharge Command	$t_{RAS.MIN(IDD)}$	45	ns
	$t_{RAS.MAX(IDD)}$	70000	ns
Precharge Command Period	$t_{RP(IDD)}$	15	ns
Average periodic Refresh interval	t_{REFI}	7.8	µs

ON DIE TERMINATION (ODT) CURRENT

The ODT function adds additional current consumption to the DDR2 SDRAM when enabled by the EMRS(1). Depending on address bits A[6,2] in the EMRS(1) a “weak” or “strong” termination can be selected. The Current consumption for any terminated input pin, depends on the input pin is in tri-state or driving 0 or 1, as Long a ODT is enabled during a given period of time.

Parameter	Symbol	Min.	Typ.	Max.	Unit	EMRS(1) State
Enabled ODT current per DQ ODT is HIGH; Data Bus inputs are FLOATING	I_{ODT0}	5	6	7.5	mA/DQ	A6=0, A2=1
		2.5	3	3.75	mA/DQ	A6=1, A2=0
		7.5	9	11.25	mA/DQ	A6=1, A2=1
Active ODT current per DQ ODT is HIGH; worst case of Data Bus inputs are STABLE or SWITCHING.	I_{ODTT}	10	12	15	mA/DQ	A6=0, A2=1
		5	6	7.5	mA/DQ	A6=1, A2=0
		15	18	22.5	mA/DQ	A6=1, A2=1

PACKAGE DIMENSION



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the MO document for complete design dimensions.