GENERAL DESCRIPTION

The **GR2DD8B-(E)512XXX and GR2DD8BD-(E)1GBXXX** modules are high speed, CMOS, dynamic random -access 512MB, 1GB ECC and Non-ECC memory modules organized in x64 / x72 configuration.

DDR2 UNBUFFERED DIMM PART INFORMATION

Part Number	Density	Organization	Component	Rank	Height
x64 NON-ECC					
GR2DD8BD-1GB800/667/533/400	1GB	128Mx64	64MX8 * 16	2	1.181 Inch
GR2DD8B-512B800/667/533/400	512MB	64Mx64	64MX8 * 8	1	1.181 Inch
x72 ECC					
GR2DD8BD-E1GB800/667/533/400	1GB	128Mx72	64MX8 * 18	2	1.181 Inch
GR2DD8B-E512800/667/533/400	512MB	64Mx72	64MX8 * 9	1	1.181 Inch

FEATURES

- Performance Range

Part Number	DDR2-800	DDR2-667	DDR2-533	DDR2-400	Unit
Speed @ CL3	400	400	400	400	Mbps
Speed @ CL4	533	533	533	400	Mbps
Speed @ CL5	800	667	533	-	Mbps
Speed @ CL6	-	-	-	-	Mbps
CL-tRCD-tRP	5-5-5	5-5-5	4-4-4	3-3-3	CK

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8 ± 0.1V
- 200Mhz f_{CK} for 400Mb, 267Mhz f_{CK} for 533Mb, 333Mhz f_{CK} for 667Mb, 400Mhz f_{CK} for 800Mb/sec/pin
- Posted /CAS
- Programmable /CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3, 4, 5
- Write Latency (WL) = Read Latency (RL) -1
- Burst Length: 4, 8 (Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Average Refresh Period 7.8us at lower then T_{CASE} 85°C, 3.9us at 85°C < T_{CASE} ≤ 95°C
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60ball FBGA – 64Mx8, 4 Banks

ADDRESS CONFIGURATION

Organization	Row Address	Column Address	Bank Address	Auto Precharge
64Mx8 (512Mb) based module	A0-A13	A0-A9	BA0-BA1	A10

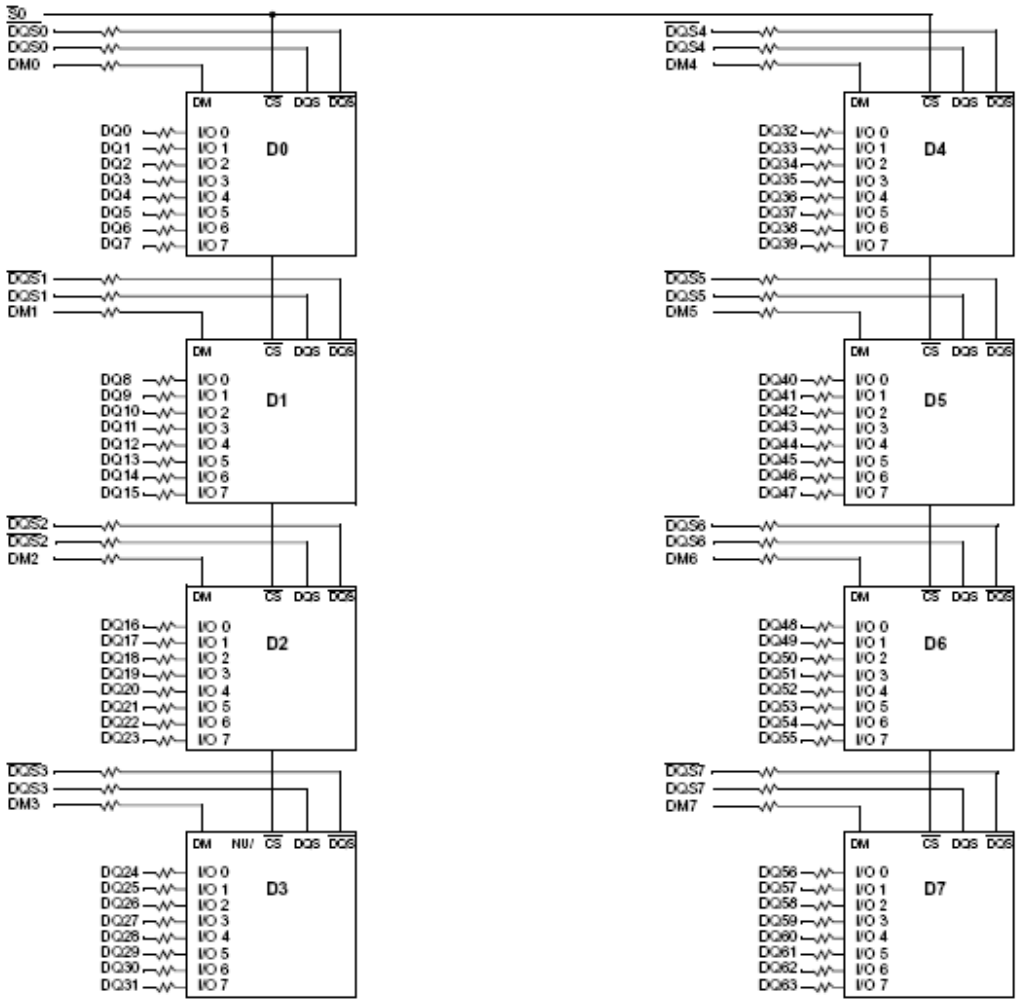
PIN CONFIGURATIONS (Front Side/ Back Side)

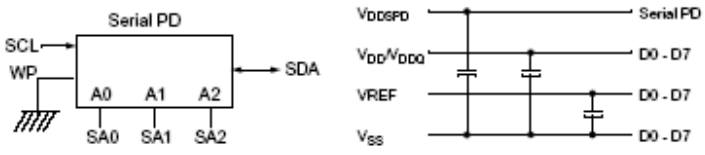
Pin	FRONT	Pin	BACK	Pin	FRONT	Pin	BACK
1	VREF	121	VSS	62	VDDQ	182	A3
2	VSS	122	DQ4	63	A2	183	A1
3	DQ0	123	DQ5	64	VDD	184	VDD
4	DQ1	124	VSS	KEY		KEY	
5	VSS	125	DM0/DQS9	65	VSS	185	CK0
6	/DQS0	126	NC	66	VSS	186	/CK0
7	DQS0	127	VSS	67	VDD	187	VDD
8	VSS	128	DQ6	68	NC	188	A0
9	DQ2	129	DQ7	69	VDD	189	VDD
10	DQ3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	DQ12	71	BA0	191	VDDQ
12	DQ8	132	DQ13	72	VDDQ	192	/RAS
13	DQ9	133	VSS	73	WE*	193	/S0
14	VSS	134	DM1/DQS10	74	CAS*	194	VDDQ
15	/DQS1	135	NC	75	VDDQ	195	ODT0
16	DQS1	136	VSS	76	/S1	196	A13
17	VSS	137	CK1	77	ODT1	197	VDD
18	NC	138	/CK1	78	VDDQ	198	VSS
19	NC	139	VSS	79	VSS	199	DQ36
20	VSS	140	DQ14	80	DQ32	200	DQ37
21	DQ10	141	DQ15	81	DQ33	201	VSS
22	DQ11	142	VSS	82	VSS	202	DM4/DQS13
23	VSS	143	DQ20	83	/DQS4	203	NC
24	DQ16	144	DQ21	84	DQS4	204	VSS
25	DQ17	145	VSS	85	VSS	205	DQ38
26	VSS	146	DM2/DQS11	86	DQ34	206	DQ39
27	/DQS2	147	NC	87	DQ35	207	VSS
28	DQS2	148	VSS	88	VSS	208	DQ44
29	VSS	149	DQ22	89	DQ40	209	DQ45
30	DQ18	150	DQ23	90	DQ41	210	VSS
31	DQ19	151	VSS	91	VSS	211	DM5/DQS14
32	VSS	152	DQ28	92	/DQS5	212	NC
33	DQ24	153	DQ29	93	DQS5	213	VSS
34	DQ25	154	VSS	94	VSS	214	DQ46
35	VSS	155	DM3/DQS12	95	DQ42	215	DQ47
36	/DQS3	156	NC	96	DQ43	216	VSS
37	DQS3	157	VSS	97	VSS	217	DQ52
38	VSS	158	DQ30	98	DQ48	218	DQ53
39	DQ26	159	DQ31	99	DQ49	219	VSS
40	DQ27	160	VSS	100	VSS	220	CK2
41	VSS	161	NC	101	SA2	221	/CK2
42	NC	162	NC	102	NC	222	VSS
43	NC	163	VSS	103	VSS	223	DM6/DQS15
44	VSS	164	NC	104	/DQS6	224	NC
45	NC	165	NC	105	DQS6	225	VSS
46	NC	166	VSS	106	VSS	226	DQ54
47	VSS	167	NC	107	DQ50	227	DQ55
48	NC	168	NC	108	DQ51	228	VSS
49	NC	169	VSS	109	VSS	229	DQ60
50	VSS	170	VDDQ	110	DQ56	230	DQ61
51	VDDQ	171	CKE1	111	DQ57	231	VSS
52	CKE0	172	VDD	112	VSS	232	DM7/DQS16
53	VDD	173	NC	113	/DQS7	233	NC
54	NC	174	NC	114	DQS7	234	VSS
55	NC	175	VDDQ	115	VSS	235	DQ62
56	VDDQ	176	A12	116	DQ58	236	DQ63
57	A11	177	A9	117	DQ59	237	VSS
58	A7	178	VDD	118	VSS	238	VDDSPD
59	VDD	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1
61	A4	181	VDDQ				

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Polarity	Function
CK0~CK2, /CK0~/CK2	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and he falling edge of /CK. An on-board DLL circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE [1:0]	Input	Active High	CKE high activates and CKE low deactivates internal signals and device input buffers and output drivers of the SDRAMs. Taking CKE low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank).
/S [1:0]	Input	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. The input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both CS*[1:0] are high, all register outputs (except CK, ODT and Chip select) remain in the previous state.
ODT [1:0]	Input	Active High	On-Die Termination control signals
/RAS, /CAS, /WE	Input	Active Low	When sampled at the positive edge of the clock, RAS*, CAS* and WE* define the operation to be executed by the SDRAM.
BA [1:0]	Input	-	Selects which internal SDRAM memory bank is activated
A [13:0]	Input	-	During Bank Activate command cycle, Address defines the row address. During a Read or Write command cycle, Address defines the column address. In addition to the column address, A10 (=AP) is used to invoke Auto-Precharge operation at the end of the burst read or write cycle. If AP is high, Auto Precharge is selected and BA[1:0] defines the bank to be precharged. If AP is low, Auto-Precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA[1:0] to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA[1:0]. If AP is low, BA[1:0] are used to define which bank to precharge.
DQ [63:0]	I/O	-	Data and Check Bit Input/Output pins.
DQS [8:0] /DQS[8:0]	I/O	Cross point	The data strobes, associated with one data byte, source with data transfer. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode the data strobe is sources by the DDR2 SDRAM and is sent at the leading edge of the data window. DQS* signals are complements, and timing is relative to the crosspoint of respective DQS and DQS*. If the module is to be operated in single ended strobe mode, all DQS* signals must be tied on the system board to VSS and DDR2 SDRAM mode registers programmed appropriately.
SA [1:0]	Input	-	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range
SDA	I/O	-	This bidirectional pin is used to transfer data into and out of the SPD EEPROM. A resistor maybe connected from the SDA bus line to VDDSPD on the system planar to act as a pull-up.
SCL	Input	-	This signal is used to clock data into the SPD EEPROM. A resistor maybe connected from the SCL bus line to VDDSPD on the system planar to act as a pull-up.
DM0~DM8	Input	-	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR SDRAM input buffers and core logic.
V_{REF}	Supply	-	Reference voltage for the SSTL-18 inputs.
V_{DDSPD}	Supply	-	Serial EEPROM positive power supply, wired to a separated power pin at the connector which supports from 1.7 Volt to 3.6 Volt.

FUNCTIONAL BLOCK DIAGRAM (GR2DD8B-512XXX)





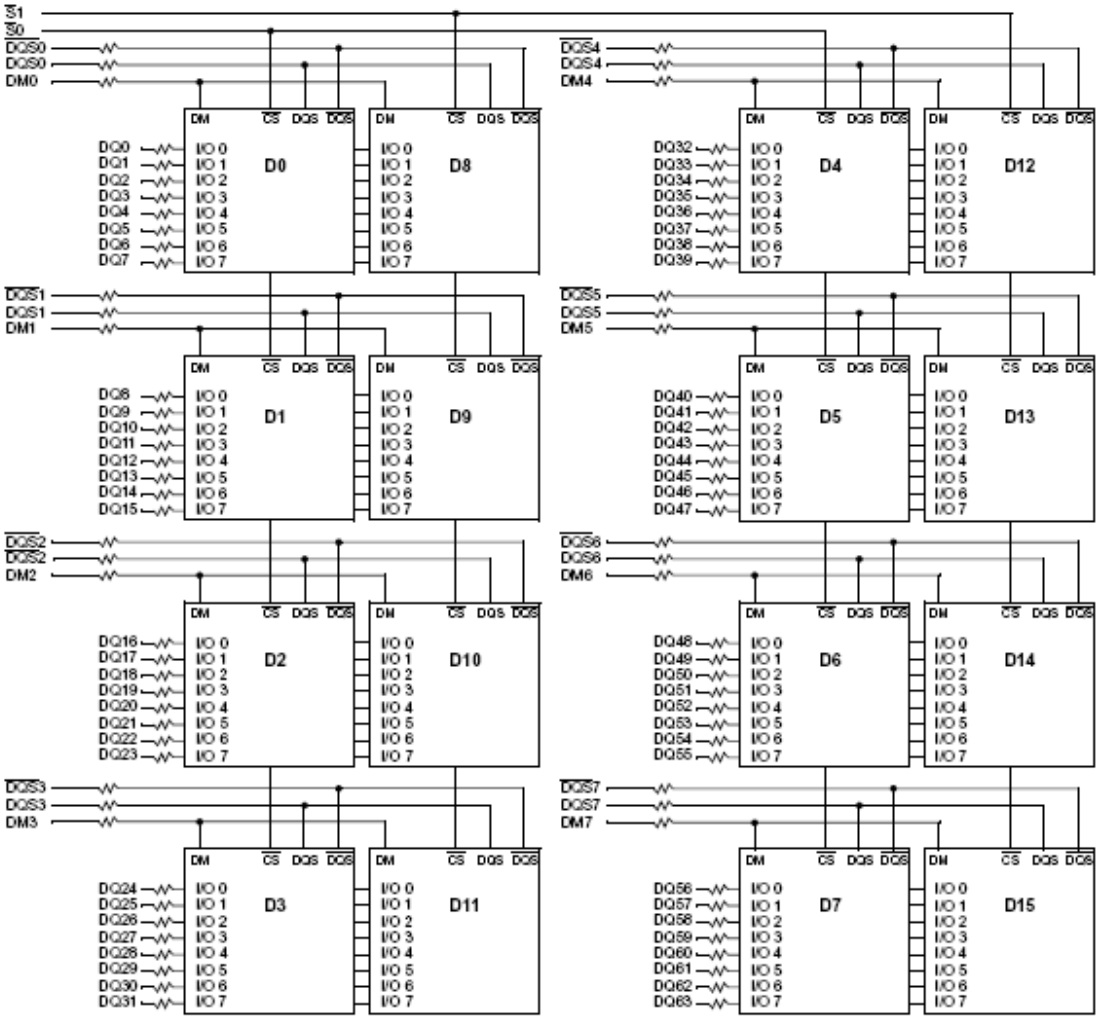
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	2 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

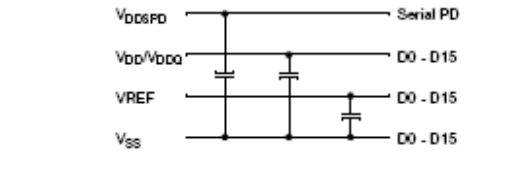
*Wire per Clock Loading Table/Wiring Diagrams

BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D7
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D7
RAS → RAS : DDR2 SDRAMs D0 - D7
CAS → CAS : DDR2 SDRAMs D0 - D7
CKE0 → CKE : DDR2 SDRAMs D0 - D7
WE → WE : DDR2 SDRAMs D0 - D7
ODT0 → ODT : DDR2 SDRAMs D0 - D7

Notes :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ±5%.
2. BAx, Ax, RAS, CAS, WE resistors : 5.1 Ohms ±5%.

FUNCTIONAL BLOCK DIAGRAM (GR2DD8BD-1GBXXX)





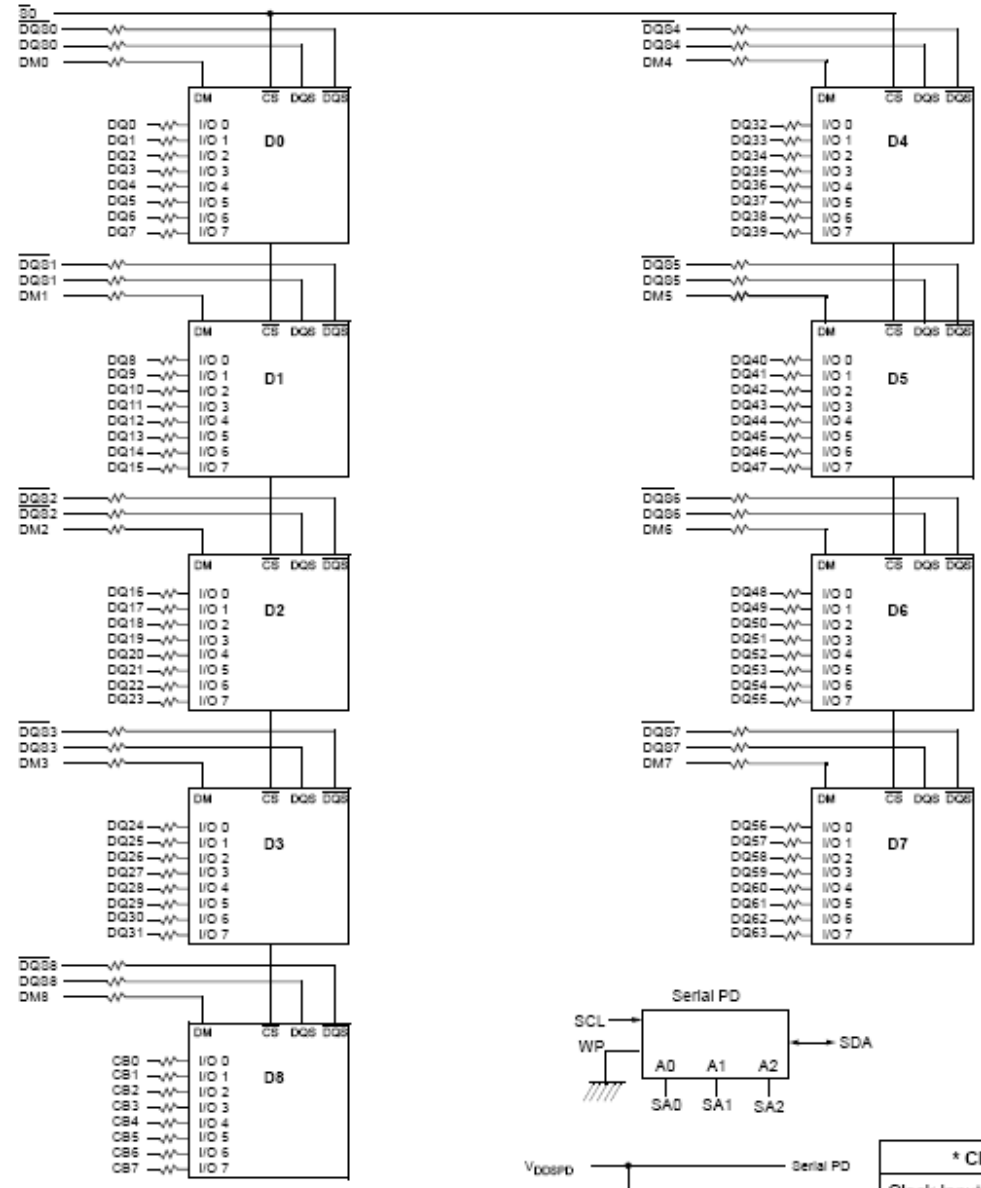
BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D15
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D15
CKE0 → CKE : DDR2 SDRAMs D0 - D7
CKE1 → CKE : DDR2 SDRAMs D8 - D15
$\overline{RAS}$ → $\overline{RAS}$: DDR2 SDRAMs D0 - D15
$\overline{CAS}$ → $\overline{CAS}$: DDR2 SDRAMs D0 - D15
$\overline{WE}$ → $\overline{WE}$: DDR2 SDRAMs D0 - D15
ODT0 → ODT : DDR2 SDRAMs D0 - D7
ODT1 → ODT : DDR2 SDRAMs D8 - D15

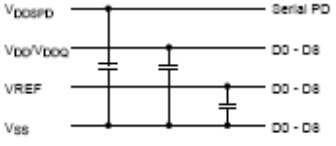
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/$\overline{CK0}$	4 DDR2 SDRAMs
*CK1/$\overline{CK1}$	6 DDR2 SDRAMs
*CK2/$\overline{CK2}$	6 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

Notes :
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3 Ohms ± 5%.

FUNCTIONAL BLOCK DIAGRAM (GR2DD8B-E512XXX)





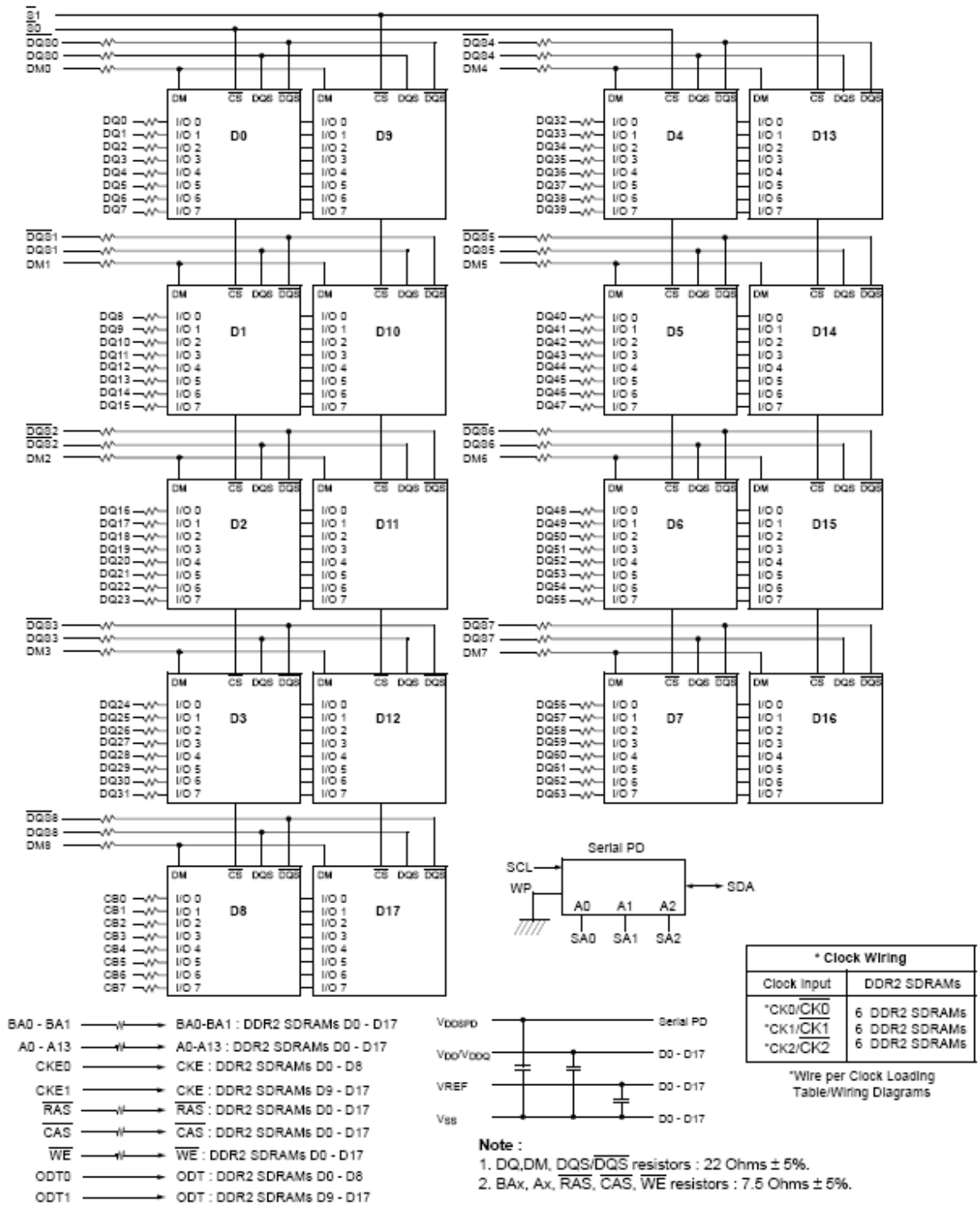
* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	3 DDR2 SDRAMs
*CK1/CK1	3 DDR2 SDRAMs
*CK2/CK2	3 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D8
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D8
RAS → RAS : DDR2 SDRAMs D0 - D8
CAS → CAS : DDR2 SDRAMs D0 - D8
CKE0 → CKE : DDR2 SDRAMs D0 - D8
WE → WE : DDR2 SDRAMs D0 - D8
ODT0 → ODT : DDR2 SDRAMs D0 - D8

Note :
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 10 Ohms ± 5%.

FUNCTIONAL BLOCK DIAGRAM (GR2DD8B-E512XXX)



* Clock Wiring	
Clock Input	DDR2 SDRAMs
*CK0/CK0	6 DDR2 SDRAMs
*CK1/CK1	6 DDR2 SDRAMs
*CK2/CK2	6 DDR2 SDRAMs

*Wire per Clock Loading Table/Wiring Diagrams

Note :

1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 7.5 Ohms ± 5%.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Limit Values		Unit
		Min.	Max.	
Voltage on any pins relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	2.3	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}	-1.0	2.3	V
Voltage on V_{DDQ} relative to V_{SS}	V_{DDQ}	-0.5	2.3	V
Storage temperature range	T_{STG}	-55	+100	° C

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING TEMPERATURE RANGE

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
DIMM Module Operating Temperature Range (ambient)	TOPR	0	+55	° C	
DRAM Component Case Temperature Range	TCASE	0	+95	° C	1 - 4

1. DRAM Component Case Temperature is the surface temperature in the center on the top side of any of the DRAMs. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. Within the DRAM Component Case Temperature range all DRAM specification will be supported.
3. Above 85 ° C DRAM case temperature the Auto-Refresh command interval has to be reduced to tREF1= 3.9us.
4. Self-Refresh period is hard-coded in the DRAMs and therefore it is imperative that the system ensures the DRAM is below 85 ° C case temperature before initiating self-refresh operation.

AC & DC OPERATING CONDITIONS

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Norm.	Max.		
Device Supply Voltage	V_{DD}	1.7	1.8	1.9	V	-
Output Supply Voltage	V_{DDQ}	1.7	1.8	1.9	V	1)
Input Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.5 x V_{DDQ}	0.51 x V_{DDQ}	mV	2)
Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3)

1. Under all conditions, V_{DDQ} must be less than or equal to VDD
2. Peak to peak AC noise on V_{REF} may not exceed ± 2% $V_{REF\ (DC)}$. V_{REF} is also expected to track noise variations in V_{DDQ}.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.

OPERATING CURRENT TABLE

512MB (64Mx8*8) MODULE

Symbol	DDDR2-800@CL5	DDR2-667@CL5	DDR2-533@CL4	DDR2-400@CL3	Unit	Note
I_{DD0}	680	600	600	560	mA	1
I_{DD1}	760	720	680	680	mA	1
I_{DD2P}	64	64	64	64	mA	2
I_{DD2Q}	280	280	240	240	mA	2
I_{DD2N}	320	320	280	280	mA	2
$I_{DD3P(F)}$	240	240	240	240	mA	2
$I_{DD3P(S)}$	96	96	96	96	mA	2
I_{DD3N}	480	440	400	400	mA	2
I_{DD4W}	920	840	720	680	mA	1
I_{DD4R}	1160	1080	880	800	mA	1
I_{DD5B}	920	880	880	840	mA	2
I_{DD6}	64	64	64	64	mA	2
I_{DD7}	1720	1440	1440	1440	mA	1

1GB (64Mx8*16) MODULE

Symbol	DDDR2-800@CL5	DDR2-667@CL5	DDR2-533@CL4	DDR2-400@CL3	Unit	Note
I_{DD0}	1000	920	880	840	mA	1
I_{DD1}	1080	1040	960	960	mA	1
I_{DD2P}	128	128	128	128	mA	2
I_{DD2Q}	560	560	480	480	mA	2
I_{DD2N}	640	640	560	560	mA	2
$I_{DD3P(F)}$	480	480	480	480	mA	2
$I_{DD3P(S)}$	192	192	192	192	mA	2
I_{DD3N}	800	760	680	680	mA	2
I_{DD4W}	1240	1160	1000	960	mA	1
I_{DD4R}	1480	1400	1160	1080	mA	1
I_{DD5B}	1240	1200	1160	1120	mA	2
I_{DD6}	128	128	128	128	mA	2
I_{DD7}	2200	1760	1720	1720	mA	1

Notes:

1. Value calculated as one module rank in this operating condition and all other module ranks in I_{DD2P} (CKE LOW) mode.
2. Value calculated reflects all module ranks in this operating condition.

512MB (64Mx8*9) ECC MODULE

Symbol	DDDR2-800@CL5	DDR2-667@CL5	DDR2-533@CL4	DDR2-400@CL3	Unit	Note
I_{DD0}	765	675	675	630	mA	1
I_{DD1}	855	810	765	765	mA	1
I_{DD2P}	72	72	72	72	mA	2
I_{DD2Q}	315	315	270	270	mA	2
I_{DD2N}	360	360	315	315	mA	2
$I_{DD3P(F)}$	270	270	270	270	mA	2
$I_{DD3P(S)}$	108	108	108	108	mA	2
I_{DD3N}	540	495	450	450	mA	2
I_{DD4W}	1035	945	810	765	mA	1
I_{DD4R}	1305	1215	990	900	mA	1
I_{DD5B}	1035	990	990	945	mA	2
I_{DD6}	72	72	72	72	mA	2
I_{DD7}	1935	1620	1620	1620	mA	1

1GB (64Mx8*18) ECC MODULE

Symbol	DDDR2-800@CL5	DDR2-667@CL5	DDR2-533@CL4	DDR2-400@CL3	Unit	Note
I_{DD0}	1125	1035	990	945	mA	1
I_{DD1}	1215	1170	1080	1080	mA	1
I_{DD2P}	144	144	144	144	mA	2
I_{DD2Q}	630	630	540	540	mA	2
I_{DD2N}	720	720	630	630	mA	2
$I_{DD3P(F)}$	540	540	540	540	mA	2
$I_{DD3P(S)}$	216	216	216	216	mA	2
I_{DD3N}	900	855	765	765	mA	2
I_{DD4W}	1395	1305	1125	1080	mA	1
I_{DD4R}	1665	1575	1305	1215	mA	1
I_{DD5B}	1395	1350	1305	1280	mA	2
I_{DD6}	144	144	144	144	mA	2
I_{DD7}	2475	1980	1935	1935	mA	1

INPUT ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

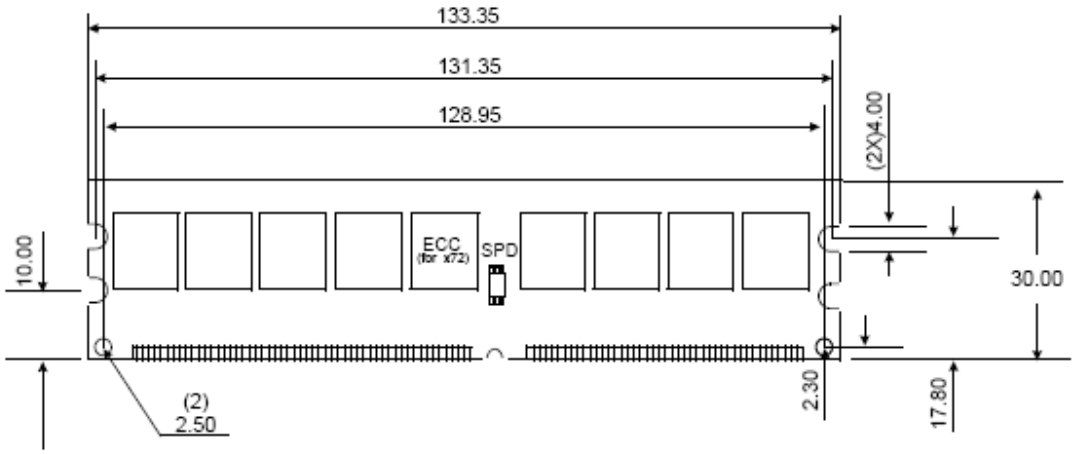
Input DC Logic Levels

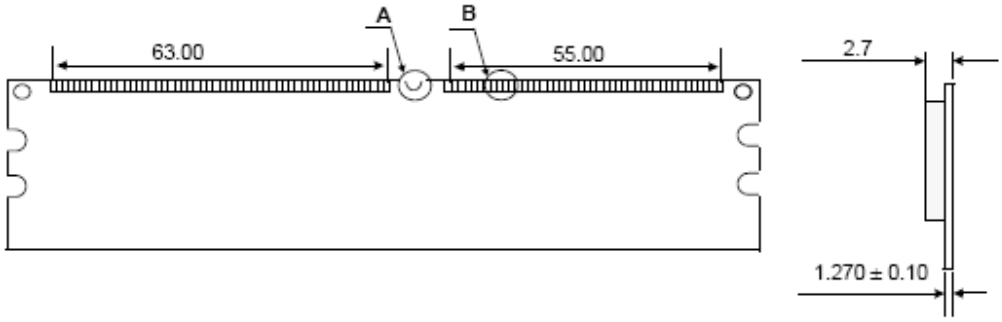
Parameter	Symbol	MIN	MAX	Units	Notes
Input High (Logic 1) Voltage	$V_{IH\ (DC)}$	V_{REF} + 125	V_{DDQ} + 300	mV	
Input Low (Logic 0) Voltage	$V_{IL\ (DC)}$	-300	V_{REF} - 125	mV	

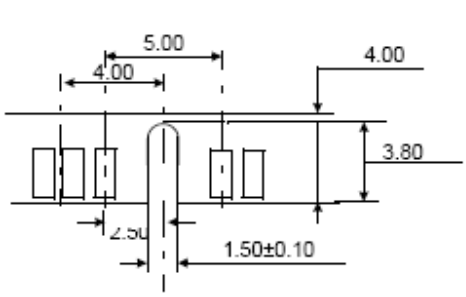
Input AC Logic Levels

Parameter	Symbol	MIN	MAX	Units	Notes
Input High (Logic 1) Voltage	$V_{IH\ (AC)}$	V_{REF} + 250	-	mV	
Input Low (Logic 0) Voltage	$V_{IL\ (AC)}$	-	V_{REF} - 250	mV	

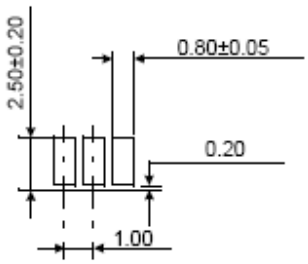
MODULE DIMENSIONS (Unit: mm): 512MB (64MX64/72) MODULE



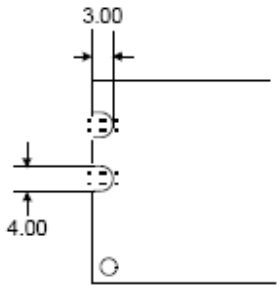




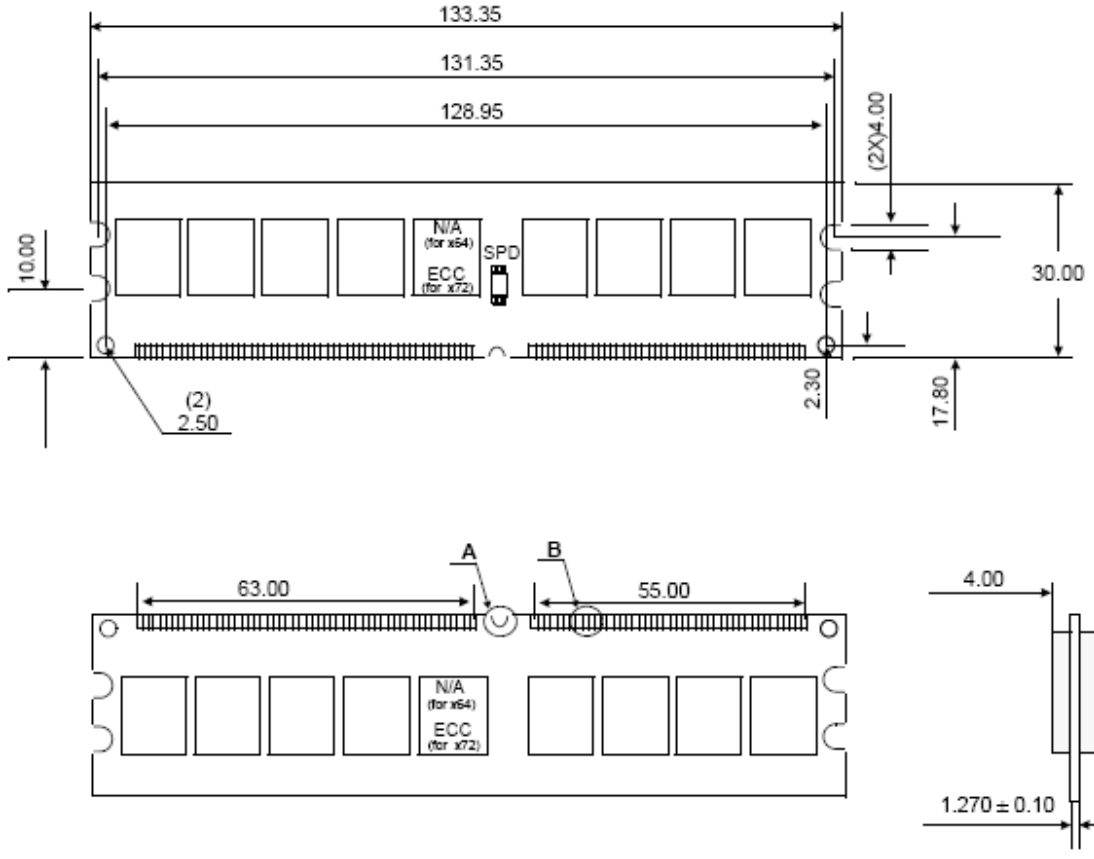
Detail A

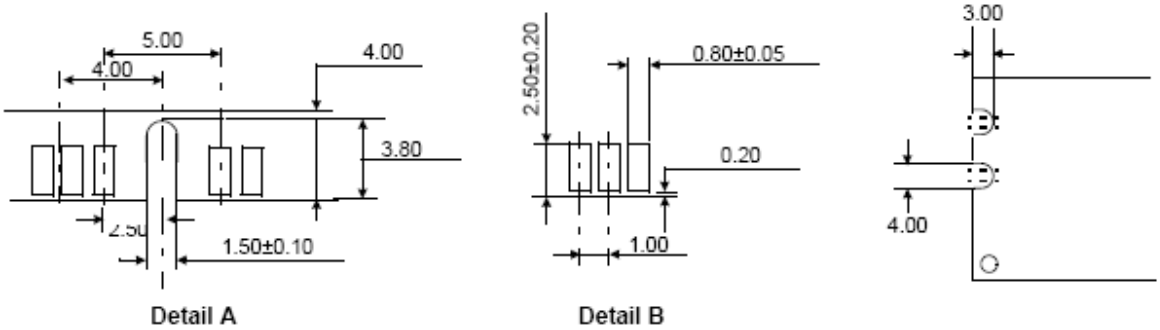


Detail B



MODULE DIMENSIONS (Unit: mm): 1GB (128MX64/72) MODULE





Detail A

Detail B